YILDIZ TEKNİK ÜNİVERSİTESİ

FEN BİLİMLERİ ENSTİTÜSÜ

PROGRAMLANABİLİR LOJİK DENETLEYİCİ (PLC) İLE BİR ENDÜSTRİYEL UYGULAMA

Elektronik ve Hab. Müh. Erkan CİRİT

F.B.E. Elektronİk Mühendislği Anabilim Dalında

hazırlanan

YÜKSEK LİSANS TEZİ

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İ Ç İ N D E K İ L E R

Şekil Listesi:

ÖZET

Bu çalışmada Spreher-such+ PLC Sestep 190 modelinin donanınımı ve yazılımı incelenmiştir. Giriş ve çıkış şekilleri yardımcı bağlantı cihazları açıklanmış olup, PRS-21 programı ile PLC nin bilgisayarla programlanması incelenmiştirrPLC ile bir endüstriyel uygulama emülasyonu gerçekleştirilmiştir.

ABSTRACT

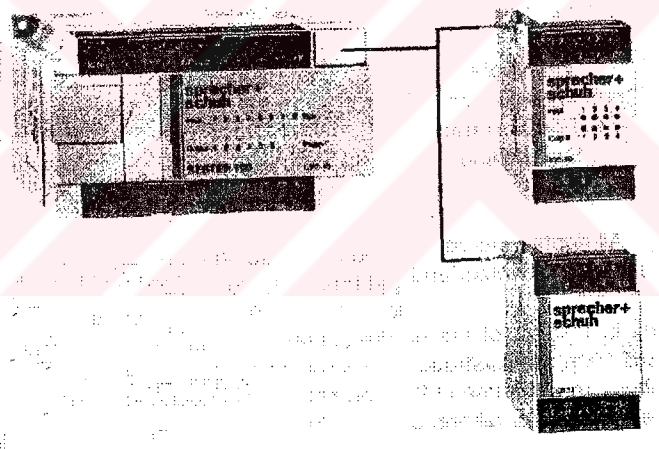
In this work I'm research hardware and software of Spreher-Schuh+ SESTEP 190 PLC models .Input and output (I/O) types described. Sotware PRS-21 program and programming PLC with PC is researched . An industrial application emulation with PLC is done.

Bölüm-I

1 - SESTEP 190 DONANIMI

1.1 Sisteme Bakış :

Sestep 190 mikro -denetleyici rölelerle yapılan kontrollere alternatiftir. Kompleks işlemlerin basit program sıralamasıyla halletmek üzere tasarlanmıştır. Ana işlem kontrol ünitesi sink/source girişli ve röle çıkışlıdır. SESTEP 190 analog veya sayısal, giriş veya çıkışlar bağlanmaya müsaittir.



Şekil - 1

ÇIKIŞLAR

Tip : Röle

Çıkış sayısı : 6

Grupları : 2x1 ve 1x4

Voltaj izalasyonu : Röle

Anahtarlama Kapasitesi

Voltaj : 250 vac, 30 VDC

Res, Akım : 3 iki röle, 4 A iki grup

Ind, Akım : 2 A (240 vac, cosf = 0,4)

Röle ömrü : $20x10^6$ (Mekanik), $100x10^3$ (elektriksel tam yükte)

Aşırı Yükleme Ömrü : Harici olarak (Eğer ihtiyaç olursa)

Durum Göstergesi : LED

I/0 noktaları (Kullanılmış) : 8, adresleri Y001... Y006

HARİCİ ÇIKIŞ (Voltaj besleme)

Voltaj : 24 VAC, ± o/o 10

Akım : 300 mA

Ripple : 200 mV max.

REAL-TİME CLOCK

Çalışma Dilmi : ± 30s /Ay

Çalışma Koruması : Yaklaşık 10 yıl

YAZILIM

Kontrol Prensibi : Çevrimsel işlem

Programlama Dilleri :

PC ile : Ladder diyagramı, komut listesi

Programlama cihazı : Komut listesi

Kullanıcı Hafızası : 3001 adım

Hafıza Tipi : Pil - korumalı RAM, EEPROM, EPROM

Yerİne getirme süresi : 6 Ms / basit komut

Girişler : 128 X001...X128

Çıkışlar : 128 Y001...Y128

Dahili Kütük : 992 C001... C0232, C0265, C1024

Özel Dahili Kütük : 32 C0233...C0264

Sabit Yükleme Kütüğü : 512 WC001...WC 512

Sayıcı/Zamanlayıcı(timer) :64 V001...V064,V0157...V0160

Yüksek Hızlı Sayıcı :1 V0065

Kütükler :831 V066...V0128,V0257...V1024

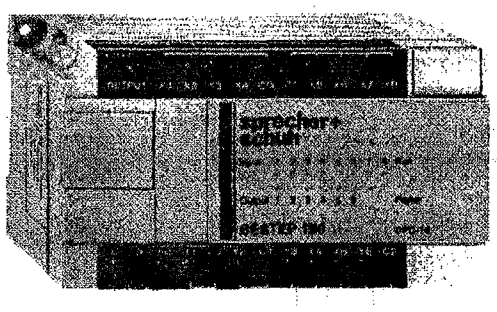
Özel Kütükler :128 V0129...V0256

Giriş Kütükleri :16 WX01...WX16

Çıkış Kütükleri :16 WY01...WY16

Seguencers :8

1.2 TEMEL ÜNİTE CPC-XX



ŞEKİL - 2

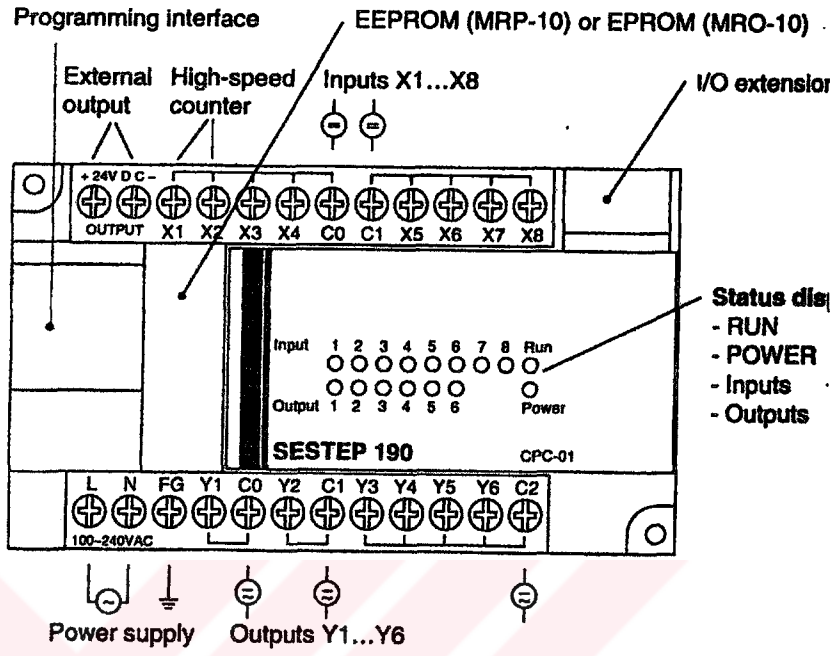
- 8 Sayısal Giriş
- 6 Sayısal Çıkış Röleleri
- Durum Göstergesi

1.2.a - Ana Ünite Çeşitleri :

CPC-01	220VAC
CPC-01 H	220VAC/2 faz sayıcı
CPC-02	220VAC/clock
CPC-02 H	220VAC/clock 2faz sayıcı
CPC-03	220VAC/EEPROM
CPC-04	220VAC/clock/EEPROM
CPC-11	24VDC/
CPC-11 H	24VDC/2faz sayıcı
CPC-12	24VCD/clock

CPC-12 H 24VDC/ clock/2faz sayıcı

1.2.b - Bağlantı Görünüşü :



ŞEKİL - 3

1.2.c-Teknik Bilgiler :

Genel Bilgiler :

Çalışma Voltajı : 100...240VAC 50/60Hz, (aralık 90 264VAC)

24VDC, (aralık 9 28VDC)

İzin Verilen Voltaj Kesilmesi : max 20 ms

Güç : 12VA

Çalışma Sıcaklığı : 10...75 C

Nem : 20 ...%90

Yalıtım Direnci : 20 M ohm 500 VDC

Koruma Sınıfı	: 1P 30
Pil Ömrü	: 10 yıl
Boyutlar	: 140mm x80mm x70mm
Montaj	: 35mm ray
Ağırlık	: 400gr

GİRİŞLER

Sayısal	: Akım giriş / Akım çıkış
Giriş sayısı	: 8, 2'li grup halinde 4 giriş
Voltaj izolasyonu	: Opto- coupler
Giriş Voltajı	: 12/24 VDC
Sayısal Sinyal 10 Seviyesi	: 0...5 VDC, 1,3 MA
Sayısal Sinyal 1 Seviyesi	: 9...28 VDC, 2,8 MA
Giriş Empedansı	: 4,3k ohm
Giriş Gecikmesi 0-1	: 12ms /24 VDC
Giriş Gecikmesi 1-0	: 12ms /24 VDC
Durum Göstergesi	: LED
I/0 Noktaları	: 8, adres X001... X008

YÜKSEK HIZLI SAYICI :

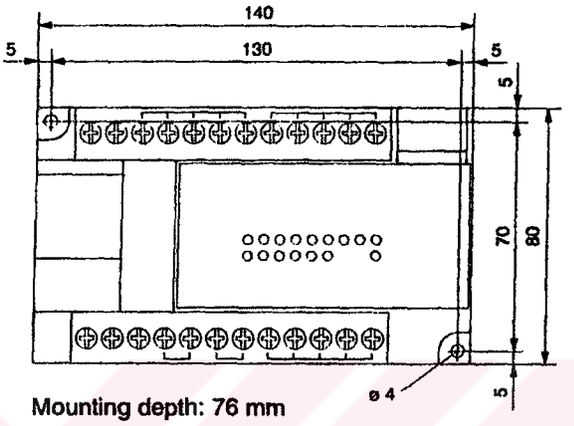
Sayıcı Girişi	: X001
Giriş Voltajı	: 24 VDC
Kontrol Voltajı Çalışma	: 9...28 VDC
Dalga Şekli	: Kare, sinüs

Darbe Genişliği : 60ms min

Frekans : 8 KHZ max

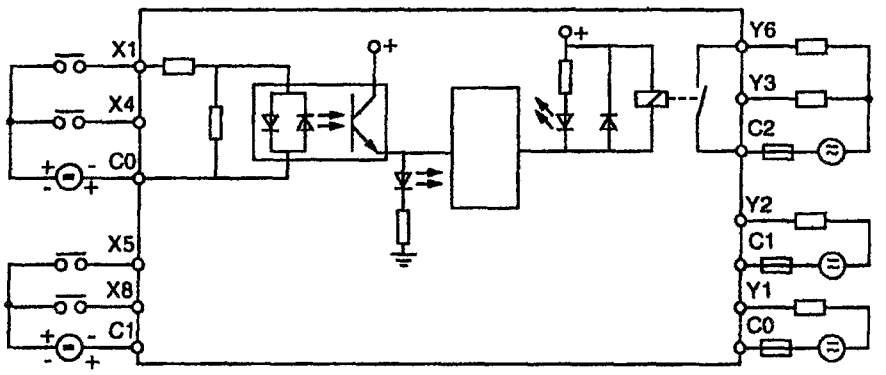
1.2. d BOYUTLAR

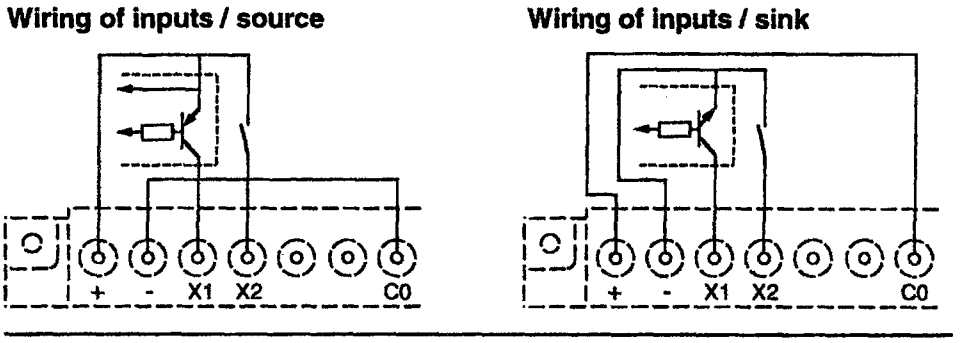
Dimensions



ŞEKİL-4

1.2. e BAĞLANTI





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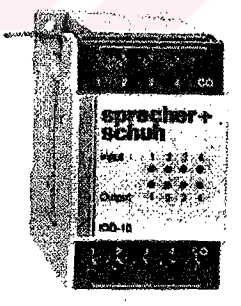
ŞEKİL -5

1.3 Sayısal Bağlantı Cihazı IDD -10



ŞEKİL -6

Bu ünite 4 giriş ve çıkış rölesi içerir. Yassı kablo ile Temel Üniteye bağlanır.

1.3. a Teknik Bilgiler

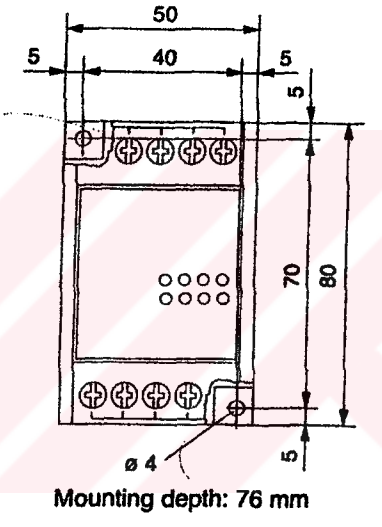
Girişler

I/0 noktası : 8 X009...X012

Çıkışlar

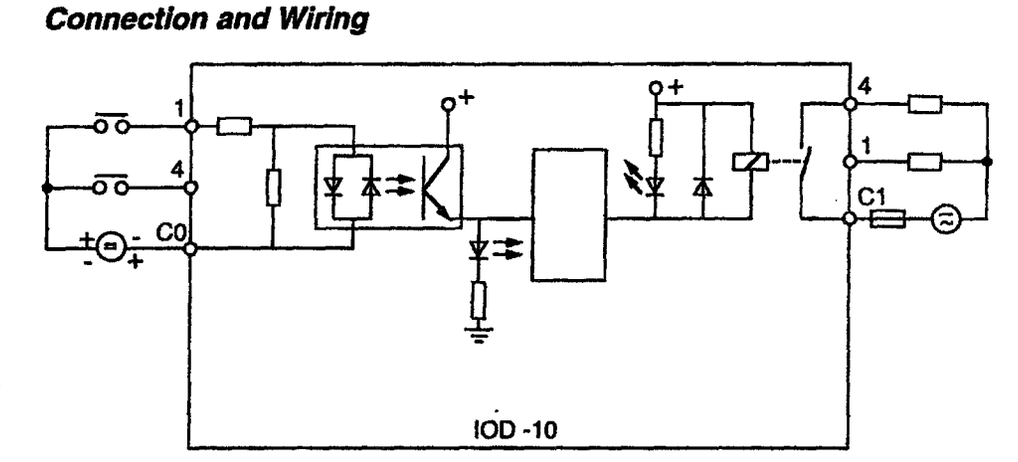
I/0 noktası : 8 Y009... Y012

1.3. b BOYUTLAR



ŞEKİL-7

1.3.C BAĞLANTI



ŞEKİL-8

1.4 - ANALOG BAĞLANTI CİHAZI IOI - 11

ŞEKİL-9

BÖLÜM - II

PROGRAMLAMA

2.1 - GİRİŞ

Kullanıcı programı ile kontrol edilir. Giriş sinyalleri sayısal olarak dahili kütklere sayıcıya aktarılır. Sonuçta ise çalışma içerisinde çıkışa etki edilir.

PC üzerinde çalışan programı üzerinden Ladder Diyagramı ile programlanır.

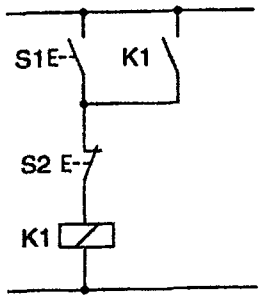
Ladder Diyagramı (LD) : Prensipte Ladder Diyagramı elektriksel devre diyagramlarını grafik programı üzerinde normalde açık kontak, normalde kapalı kontak ve bobin elemanları gibi göstererek kullanılır. Her elemanın adresi üstünde yazılıdır.

Komut Listesi (ID) : Komut listesi elektriksel diyagramı tanımlayacak şekilde belirlenir. Her komut adı ile grafik sembollü LD geçiş yapılabilir. Her elemanın adresi aynı satırda komutun sağına yazılır. Program çalışma esnasında X girişi bir program tararıncaya kadar aynı durumda kalır. İç kütükler C, çıkışlar Y ve kütüklerin içerikleri program taranırken yenilenir. Fakat fiziksel çıkışlar açık veya kapalı duruma taranan durumdaki cevabına göre konum değiştirir.

2.2 - Güvenli Programlama :

Konvansiyonel kontrol sistemlerinde, personel tarafından kullanılacak ACİL-DURMA ile direk besleme hattı kesilir.

Aşağıdaki örnekte tutma mekanizması (Acil Durma) için PLC için uygulamı görülmektedir.

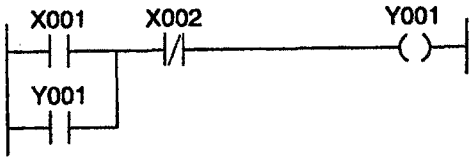


ŞEKİL-10

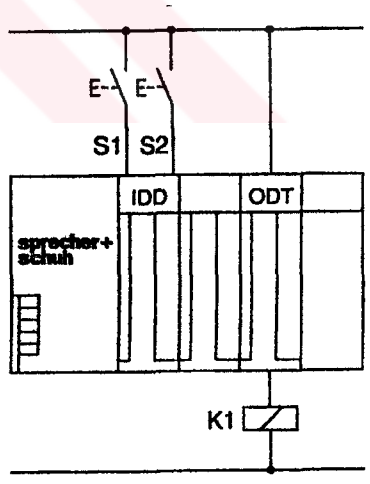
Devre Açıklaması : Konvansiyonel teknolojide, DURMA (kapatma) anahtarı (S2) normalde kapalıdır. Herhaaangi durma anında (S2) den dolayı kontaktör (K1) konum değiştirir.

Ladder Diyagramında yukarıda anlatılan işlemi gerçekleştirmeye çalıştığımızda iki çözüm çıkar. Bunlardan birincisi topraklama güvenliği açısından yanlıştır.

a) Birinci Çözüm:



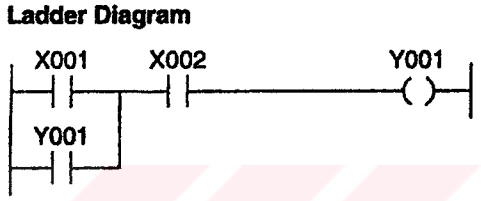
ŞEKİL-11



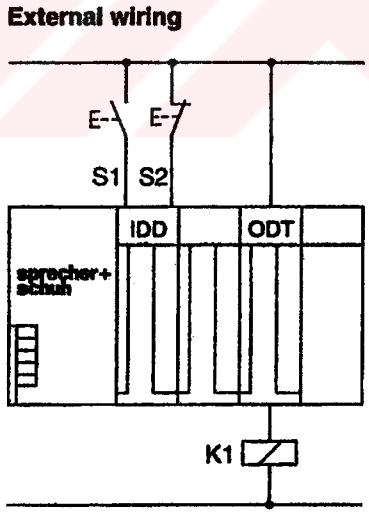
ŞEKİL-12

Devre diyagramından direk kopyalanarak gerçekleştirilmiştir. Arızasız çalışma durumunda problemsizce çalışır. Fakat S2 anahtarının bağlantısında kopukluk olması tutma-devresinde kontak törün konum değiştirmemesine neden olmakta, bu yüzden sakıncalıdır.

b) İkinci Çözüm (Doğru Çözüm)



ŞEKİL -13

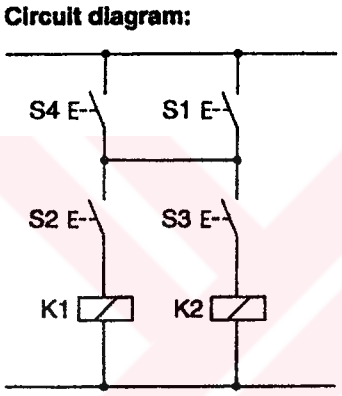


ŞEKİL - 14

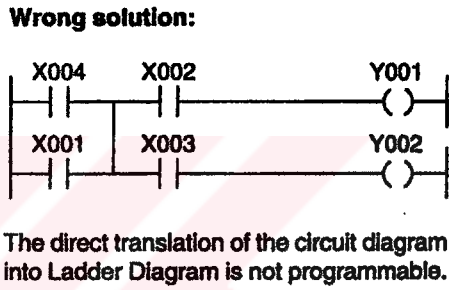
Kapatma (S2) anahtarı lojik 1 durumundadır. S2 normalde kapalı kontaktır, bu yüzden X2 seviye olarak yüksek durumdadır. Ne zaman S2 anahtarına basılırsa, devre kesilir, tutma durumu konum değiştirir. Bu mantıktan dolayı S2 anahtarı ile ilgili devrede kopukluk olması kontaktörün konum değiştirmesine neden olur.

2.3 - Programlama İçin Notlar :

Röle devreleri ve PLC üzerinde çalıştırılması üzerine bazı mantık farklılıkları vardır. Devre diyagramın, Ladder Diyagramı ile direk programlanması her zaman doğru çözüm değildir. Aşağıda buna ait bir uygulama bulabilirsiniz.

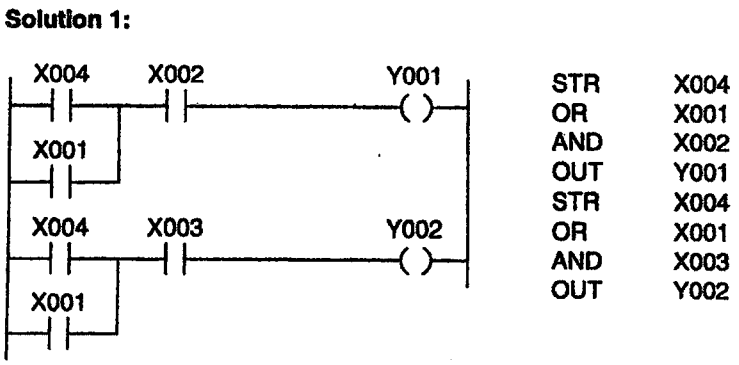


ŞEKİL -15



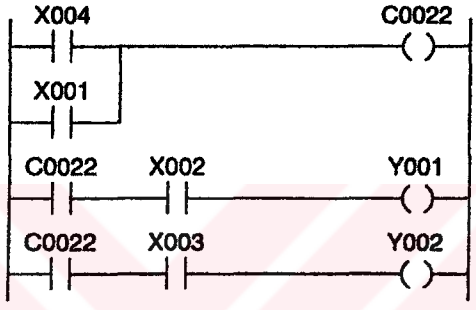
ŞEKİL -16

Doğru Çözümler aşağıdadır.



ŞEKİL -17

Solution 2:
Ladder Diagram using the internal register C0022.




```
STR   X004
OR    X001
OUT   C0022
STR   C0022
AND   X002
OUT   Y001
STR   C0022
AND   X003
OUT   Y002
```

ŞEKİL -18

2.4 - VERİ HAFIZA YERİNİN AÇIKLAMASI

Eleman	No	Aralık
Giriş	128	X001...X128
Çıkış	128	Y001...Y128
İç Kütük	992	C001...C0232
		C265...C1024
Özel İç Kütük	32	C0233...C0264

Sabit Kütük	512	WC001...WC512
Sayıcı / Zamanlayıcı	64	V0001...V0064
	4	V0157...V0160
Yüksek Hızlı Sayıcı	1	V0065
Kütükler	831	V0066...V0128
		V0257...V1024
Özel Kütükler	128	V0129...V0256
Giriş Kütüğü	16	WX01...WX16
Çıkış	16	WY01...WY16
Sekansiyer	8	S 101...S 116
		S 801...S 816

- V, WX VE WY 16 bitlik kütüktür.

2.4.1 - Özel İç Kütüklerin Fonksiyonları

C0233 Ne zaman aktif olarak set edilirse, çıkışlar OFF olur.

C0234 Ne zaman aktif / aktif -değil olursa hızlı sayıcı başla / dur konumunda olur.

C0235 Aktif olduğunda, V0065 (Hızlı-sayıcı) kütüğü temizlenir.

C0236 Programlama cihazı ile ON/OFF yapılır. Ne zaman ON olursa bütün çıkış ve giriş kütükleri kısa süre bobin olarak kullanılır.

C0237 ON olduğundan işlemci aktifliğini yitirir.

C0238 ON olduğunda sayıcı /zamanlayıcı cihaz kapatıldıktan sonra tanımlanır.

C0239 Programlayıcı tarafından OFF yapıldığında CPU durma durumunda olup çıkışlar aktif durumda değildir.

C0240 Programlayıcı tarafından OFF yapıldığında, bütün kütükler yeniden belirlenir. (CPU stop made veya voltaj hatası)

Aşağıda belirtilen kütükler kullanıcı tarafından set ve reset edilir. Bunların bulunduğu konum uygulama programı tarafından kullanılır.

C0241 No carry bit (Taşıyıcı yok)

C0242 Carry bit (Taşıyıcı)

C0243 Sıfır (Zero)

C0244 Hata-ERR (Errer bit)

C0245 Ever OFF-Özel registerler her zaman OFF

C0246 0,1 saniye çevrim zamanı

C0247 0,4 saniye çevrim zamanı

C0248 0,8 saniye çevrim zamanı

C0249 Bu özel kütük ON olduğunda, hafızada hata olduğunu gösterir.

C0250 On olduğunda Reset işleminin tam çalışmadığını gösterir.

C0251 Bu kütük ON olduğunda, giriş ve çıkış modüllerinde hatayı belirtir.

C0252 Rezerve edilmiş.

C0253 Bu kütük ON olduğunda Reset işlemi güç hatasından dolayı gerçekleşmiş olduğunu belirtir.

C0254 Rezerve

C0255 Çalışma bayrakları.

C0256 Şifre Bayrağı ON : Şifre var OFF : Şİfre yok

C0257 Rezerve

C0258 Ayarlama bayrağı ON ise birinci program taranır off ise ikinci program taranır.

C0259 On olduğunda, ennerjili elemanlar çalıştırılmaz tarama zamanı azaltılır.

Aşağıdaki kütükler kullanıcı programı ile SET/RESET edilir.

C0260 ON olduğunda analog modüle ulaşır.

C0261 Hızlı sayıcı seçilir.

OFF-Tek faz sayıcı ON-Çift faz sayıcı

C0262 Hızlı sayıcının yönü seçilir.

C0261 : OFF C0262 : OFF İncremental Sayıcı

C0261 : OFF C0262 : ON Decremental Sayıcı

C0263 Yazma koruma bayrağı

OFF ise- clock- saat'a yazma koruması

ON ise- saat set edilir.

C0264	C0262 : OFF	C0262 : ON
V0065>V0161	ON	OFF
V0065<V0161	OFF	ON
V0065=V0161	ON	ON

2.4.2 - Özel Kütüklerin Fonksiyonları :

V0129

V0130 - Eklenmiş giriş modülü

V0131 - Eklenmiş çıkış modülü

V0132 - Kullanıcı hatasından adres

V0133 - Rezerve

V0134 - Eleman adresleri geçerli değer dışında

V0135 - Enerji hatası

V0136 - Çalışma modu 1: STOP 2: RUN 4: HATA

V0137 - Rezerve

V0138 - Program versiyonunu belirler

V0139 - Girilen yanlış şifreleri sayar

V0140 - Birinci eleman gösterge

V0141 - İkinci eleman gösterge

V0142 - Üçüncü eleman gösterge

V0143 - Dördüncü eleman gösterge

C0144 - Rezerve

C0145 - Çıkış retentive alanda YXX

C0146 - İç kütükler retentive halde

C0147 - Rezerve

C0148 - Rezerve

C0149 - Hafta günleri (1= pazartesi 7= pazar)

V0150 - Saat

V0151 - Dakika

V0152 - Saniye

V0153 - Yıl

V0154 - Ay

V0155 - Gün

V0156 - Dinlenme bölümü

V0157 -

V0160 - Zamanlayıcı 0.01s bazında

V0161 - İlk değer (preset) Kütüğü hızlı sayıcı için

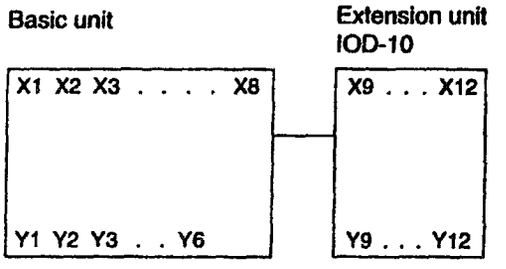
V0161 -

V0256 - Rezerve

2.5 - ADRESLEME

Temel ünite ile Digital bağlama ünitesi 10D-10'un adreslemesi :

Temel ünite sekiz giriş ve sekiz çıkış adresli olup, sadece altı çıkış fiziksel olarak kullanılır. İki çıkış dahili kütük olarak kullanılır. Eklenen giriş ve çıkış adresleri dokuzdan başlar.



Şekil - 19

Analog bağlantı ünitesinin temel ünite adreslenmesi:

Analog bağlantı ünitesi C0260 kütüğü aktif edilerek kullanılır böylece bu ünite ilk dört adresi kullanır. (WX01.. WX04, WY01..WY04)

2.6 - YÜKSEK HIZLI SAYICI

X001 sayıcı girişi olarak kullanılır. Bazı ünitelerde iki fazlı giriş bulunmakta olup, X002 ikinci faz girişidir.

Teknik Veriler :

Giriş	: X001
İkİncİ faz giriş	: X002 (Opsiyon)
Giriş voltajı	: 24 VDC
Kontrol voltajı ON	: 9...28 VDC
Kontrol voltajı OFF	: 0... 5 VDC
Sinyal şekli	: Kare, Sinüs

Darbe genişliği : Min. 60µs

Frekans : Max. 8KHz. (5KHz iki faz için)

Sayıcı kütüğü : V0065 (16 Bit.) 0...65535

Önyükleme kütüğü : V0161 (16 Bit.) 0...65535

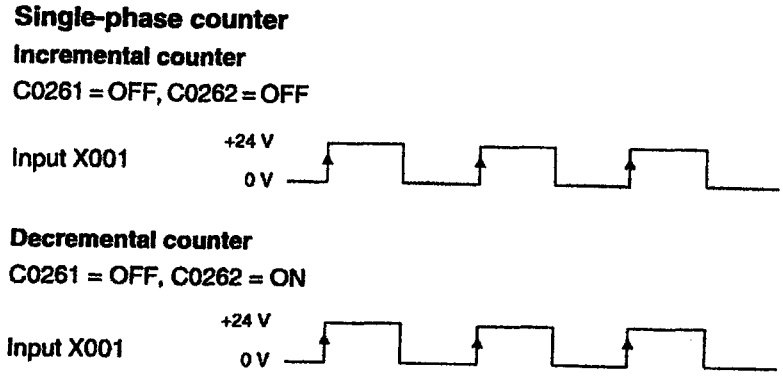
İç kütükler :

C0234	Erable	ON Sayıcı Aktif
		OFF Sayıcı Aktif Değil
C0235	Reset	ON : Counter Reset, V0065 = 0,C0265 = OFF
C0261	Sayıcı Seçimi	OFF = Tek Faz
		ON = İki Faz Sayıcı
C0262	Sayıcı Yönü	OFF = Artan Sayıcı
		ON = Azalan Sayıcı
C0264	Sinyal Karşılaştırıcı	(Bkz. Giriş açıklaması)

Tek Faz Sayıcı

a) Artan Sayıcı (C0261 = OFF, C0262 = OFF)

GİRİŞ



Şekil - 20

b) Azalan Sayıcı C0261 = OFF C0262 = ON

GİRİŞ

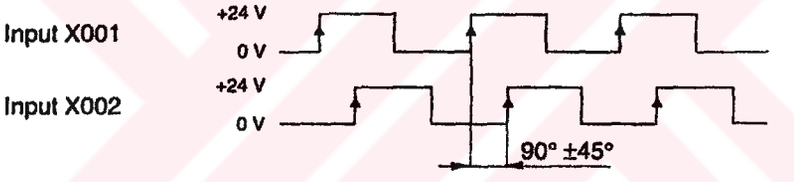
Decremental counter
C0261 = OFF, C0262 = ON

Şekil - 21

İki Faz Sayıcı :

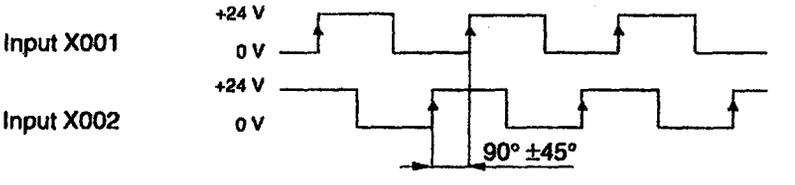
İki fazlı sayıcıda, her giriş fazı arasında 90° faz farkı vardır. X001 veya X002 fazının önce gelmesine göre artan ve azalan sayıcı olur.

2 phase counter (option)
Incremental counter
C0261 = ON, C0262 = inactive



The content of the counter register is increased by one, if the edge at input X002 in relation to the edge at input X001 is behind by 90°.

Decremental counter
C0261 = ON, C0262 = inactive



The content of the counter register is decreased by one, if the edge at input X002 in relation to the edge at input X001 is in front by 90°.

(programming example, see page 3.83)

Şekil - 22

2.7 - REAL TİME CLOCK

SESTEP 190 dahili gerçek zamanı gösteren saate sahiptir. Zaman, gün için gerçek zaman özel kütüklerine sahiptir.

V0149 - haftanın günü [1...7] 1= pazartesi 7= pazar

V0150 - saat [0...23]

V0151 - dakika [0...59]

V0152 - saniye [0...59]

V0153 - yıl [0...99]

V0154 - ay [1...12]

V0155 - gün [1...31]

Özel Dahili Kütükler :

C0263 - yazmaya karşı korumalı bayrak

Kütük = OFF : Çalişma modunda özel kütükler gerçek zamana göre tazelenir. Özel kütüklere yazımaya karşı korumalı.

Kütük = ON : Özel kütüklere yazma işlemi yapılır. Kütüklere yazılan değerler gerçek zaman kütüklerine aktarılır.

Saatin Ayarlanması :

- C0263 ON Yapılır.
- Zaman, gün ve haftanın günü özel kütüklere yazılır.
- C0263 OFF Yapılır.

2.8- KOMUTLARIN ÖZETİ

Ladder Diyagram	Komut Adı	Fonksiyonu
OUT	Çıkış	Mantıksal operasyon sonucu Y ve C çıkışlarında belirir.
STR	Saklama	X,Y,C, veya S için normalde açık kontağı için lojik başlangıç.
STR NOT	Saklama Evriği	X,Y,C, veya S için normalde kapalı kontağı için lojik başlangıç.
AND	VE	X,Y,C veya S'nin normalde açık kontağı ile ardışıl lojik iletim
AND NOT	VE-EVRİK	X,Y,C veya S'nin normalde kapalı kontağı ile ardışıl lojik iletim.
OR	VEYA	X,Y,C veya S'nin normalde açık kontağı ile paralel lojik işlem
OR NOT	VEYA-EVRİK	X,Y,C veya S'nin normalde kapalı kontağı ile paralel lojik işlem.
AND STR	VE SAKLA	X,Y,C veya S elemanları ile paralel iki bloğun ardışıl iletimi
OR STR	VEYA SAKLA	X,Y,C veya S elemanları ile iki ardışıl bloğun paralel iletimi
F-05-DIFD	Pozitif Kenar Hissetme	Ardışıl iletimde pozitif kenar hisseder. Sinyal OFF'dan ON'a geçtiğinde kontağı bir çevrim boyunca ON olarak set eder.
F-06-DIFF	Negatif Kenar	Ardışıl iletimde negatif kenar hisseder Hissetme sinyal OFF'dan ON'a geçtiğinde kontağı bir çevrim boyunca ON olarak SET eder
V000N	Sekansiyer	Ssekansiyer ile V1... V8 kütüklerinin normalde-

		açık, normalde-kapalı olarak set edilmesini sağlar
TMR ET PT	Açmada zaman	EN=ON olduğunda zamanlama elemanı gecikme elemanı 100ms lik adımlarla set redilen değere sayar. RS=ON → ET=0
CNT CV PV	Artan Sayıcı	Artan sayıcıda CLK girişine gelen sinyali pozitif kenarında, bulunan değere1ekler. RS=ON → CV =0
F-16-CNT	16Bit. Artan	DIR=ON olduğunda artan, DIR=OFF
	azalan sayıcı	Azalan sayıcı olarak çalışır
F-00-END	Program sonu	F-00 komutu program sonu olduğunu belirtir. Bunun sonucunda 0 nolu adresse döner
F-01-MCS	Anadevre	F-01 komutu ana fonksiyonel devreye başlangıcı başlangıçtır. EN=ON olduğunda F-01 ile F-02 arasındaki komutlasr çalıştırılır EN=OFF olduğunda, F-01 ile F02 arasındaki komtlar çalışmaz ve çıkışlar ile kütükler OFF durumundadır
F-02-MCS	Ana Devre	Ana devrenin bitişini belirler, çıkışlar Dönüşü üzerinde bir etkisi yoktur
F-03-JCS	Sıcrama (Jump)	EN=ON oldoğunda F-03 ile F04 devresine başlangıç arasındaki komutlar çalıştırılır.
F-04-JCS	Sıçrama (Jump)	Sıçrama devresinin bitişini belirler.
F-07=SKIP	SKIP'e başlangıç	EN=ON
F-08-ENDS	SKIP bitişi	SKIP'in bitişini belirler
F-09w SWAP	16Bıt.swap	L Byte (R6'in) içeri H byte yerleştirilir.

F-10W SFR	16Bıt. Kütük	Pozitif kenarda CLK girişi ile çiftyönlü içeriği bir yöne bırakılır
SHFT	kaydırma (shıft)	RST=ON → RE6=0
F-11XFER	8Bit.Transfer	FRM kütüğünün içeriği (L byte.) TO FRM kütüğünün L byte'na kopyalanır.
F-11wXFER	16Bit.Transver	FRM kütüğünün içeriği TO FRM kütüğüne kopyalanır.
F-12 BCD	8Bİt. binary BCD'ye	B kütüğünün (Lbyte) içeriği BCD B den BCD'ye çevrilerek BCD kütüğüne kopyalanır.
F-12 w BCD	16 bin binary'den BCD'ye	B'nin içeriği BCD'ye çevrilir ve BCD B içerik BCD'ye kopyalanır.
F-13-ADD	8 bit toplama	TO kütüğünün (Lbyte) içeriği IN TO IN kütüğünün (Lbyte) içeriğine eklenir. Sonuç TO+1 nolu kütüğü eklenir.
F-13w-ADD	16 bit toplama	TO içeriği IN kütüğü içeriği ile toplanır ve sonuç TO IN TO+1 nolu kütüğü yazılır.
F-14-SUB	8 bit çıkarma	SB kütüğünün Lbyte' ı FR kütüğü nün Lbyte' nın SB FR içeriğinden çıkarılır Sonuç SB+1 adresli kütüğe kopyalanır.
F-14w-SUB	16 bit çıkarma	SB nin içeriği, FR'nin içeriğinden çıkarılır. Sonuç SB+1 adresli kütüğe kopyalanır.
F-15-CMP	8 bit karşılaştırma	IN Lbyte'nın içeriği TO ile karşılaştırılarak =,<veya> olduğu anlaşılır.
F-15w-CMP	16 bit karşılaştırma	IN kütüğünün içeriği TO kütüğü ile karşılaştırılarak =,<> olduğu anlaşılır.
F-17-BIN	8Bit BCD	BCD kütüğü (L Byte) BCD değeri BCD den

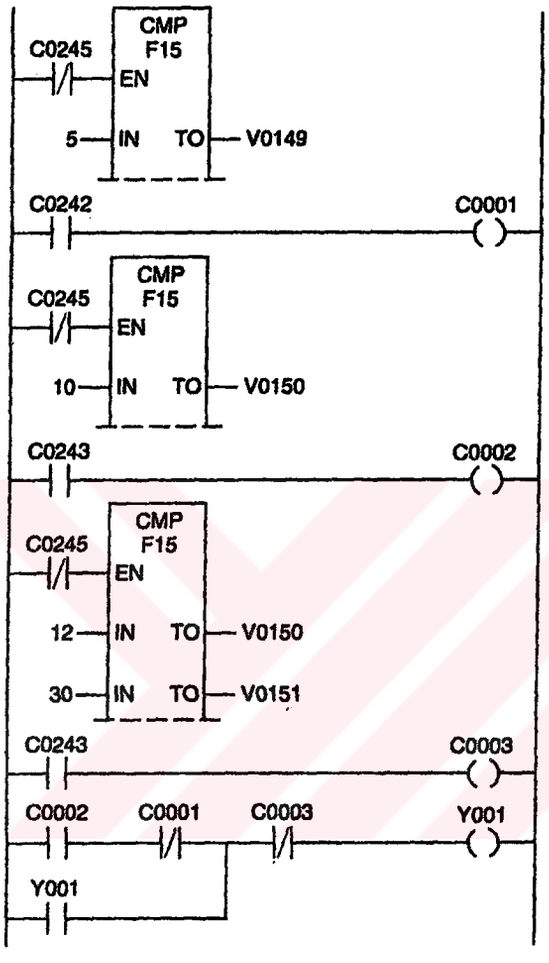
		binnary Binnary olarak B(L byte) kütüğüne Kopyalanır.
F-17w-BIN	16Bit BCD	BCD kütüğündeki BCD değer den Binnary binnary'ye çevrilir ve BCD B kütüğüne saklanır
F-18wMUL	Çarpma	MR'nin içeriği MN içeriği ile MN MR çarpılır ve sonra MN+2,MN+1 kütüklerine kaydedilir
F-19w-DN	Bölme	DN+1 ve DN içeriği DR'ye DN DR bölünür ve sonuç ON+3veDN+2 kütüğüne kopyalanır

2.9 - REAL TIME SAAT PROGLAMLAMA ÖRNEĞİ

6. Real time clock

A device should be switched on every day, with the exception of Saturday and Sunday, between 10.00 and 12.30.

Ladder Diagram of the programming software PRS-21:



On Saturdays and on Sundays C0001 is switched on.
Week-day register V0149 > 5

At 10.00, C0002 is switched on.
Hour register V0150 = 10

At 12.30, C0003 is switched on.
Hour register V0150 = 12
Minute register V0151 = 30

By linking the internal registers, the desired functionality is programmed.

For further information about the real time clock, see page 3.15

Sekil 23

BÖLÜM- III

PC ile PROGRAMLAMA

3.1 - GİRİŞ :

PRS - 21 Programı PC ile programı geliştirme, test etme yazılımıdır. Kullanıcı programı değiştirme, test etme ve saklama için çok basit programdır. Açık menü klavuzu ve yardımı minumum sürede öğrenmeyi sağlar. <F9>tuşu yardım metnin gelmesine yardımcı olur.

RRS - 21 Programı off-line yapıda olup, program içeriği direk olarak SESTEP 190 CPU'ya iletilmez. Her değişiklikten sonra CPU'ya tekrar program yüklenmektedir. RRS - 21 ile PLC durma ve çalışma moduna alınabilir.

Genel Notlar :

- Kullanıcı rahatlıkla Ladder Diyagramında programını hazırlar. <CTRL> + <B> ile komut listesini görmek için pencere açılır.
- SESTEP 190 için maksimum 3001 adımlı program yazılmalı.

3.2 - SİSTEM KONFİGRASYONU:

- IBM XT/AT veya uygun bilgisayarda
- 3 ½ Disket sürücü
- Grafik kartı Hercule E6Aveya V6A olmalı.
- RS232c Seri portu olmalı
- DOS 3. 3 veya yüksek versiyon bulunmalıdır.

3.3 - Program Entalasyonu :

3.3. a Hardiske Yükleme :

1- Program disketten kendinize bir adet kopya yapınız.

2- Program disketini disket sürücüye takınız.

3- <Drive> : install <Enter> (Program enstalasyonu başlar)

4- PRS-21 Programı alt dizine kopyalanır.

3.3. b Veri transferi SESTEP 190 PC

Veri transferi ara kablosu üzerinden gerçekleşir. SESTEP 190 CPU'ya ve PC'de (Com1-Com2)

seri portuna bağlanır.

3.4 - RRS-21 ile Programlama :

PRS-21 de Ladder Diyagramı, komutlar, değişkenler ve farklı dosyalar mevcuttur.Uzantılarına göre bu dosyaların açıklaması aşağıdaki gibidir.

LDD	Ladder Diyagram	Back - up alındığında
LBX	LDD Dosya back - up	Ladder Diyagramı değiştiğinde üstüne yazılırsa
REM	Konut	Saklandığında
RBK	Backup REM dosyası	
FRC	Değişken listesi ve içeriği	
RTP	"View Variable List" modunda değişken listesi	
LST	Printer dosya içeriği	
HEX	EPROM'a yazılmış bilgiler	
BIN	Kullanıcı program Ladder diyagramı ile	

Anahtar Tuşların Fonksyonları :

<F7> Nümerİk değerleri veya zaman formatındaki değişkenler (binary,hex,octal,decimal,time) listelenir.

<F8> Menü ile mevcut kullanıcı programları listelenir.

<F9> Herhangi bir anda yardım metnini çağırır.

<F10>

<Alt> + <E> Edit - View List ile değişkenlerin ekranda gösterilmesi veya gösterilmemesini sağlar.

<CTRL>+ <B>Ladder diyagramı ile komut listelerinin görünmesini sağlar.

<Del> Eleman yada yolların silinmesini sağlar.

<Ins> Yolların eklenmesini sağlar.

<Enter> F10 ile seçilen komutların kabul edilmesini sağlar.

<ESC> Girilen değeri iptal etmede kullanılır.

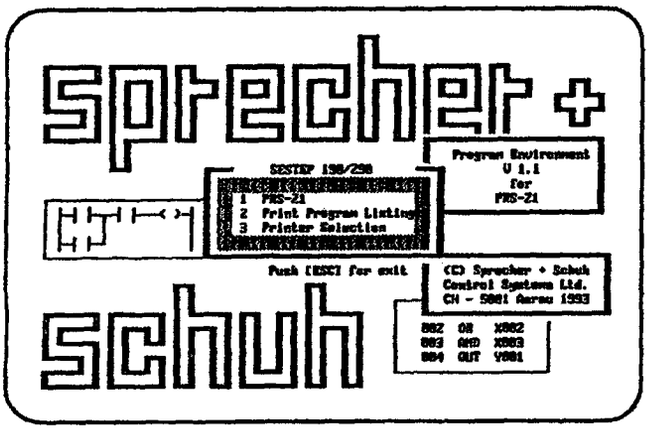
<PgUp> Kullanıcı programında aşağı satırlara inmeyi sağlar.

<PgDn> Kullanıcı programında yukarı satırlara çıkmayı sağlar.

3.5 - Programa Başlangıç :

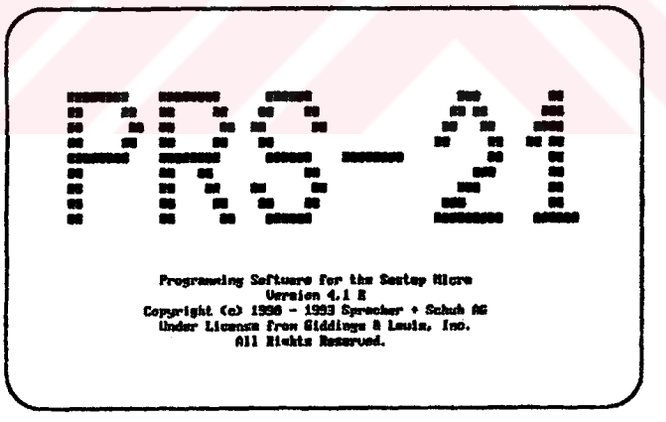
Programa başlamak için [Start] <Enter> ile başlanır. Ekranda PRS-21 Programi görünür ok tuşları ile menüden seçim yapılır ve <Enter> ile kabul edilir.

1. PRS - 21 (PC yazılımına başlangıç)
2. Programı basma.
3. Yazıcı seçimi.



Şekil - 24

PRS - 21 Seçilerek <Enter> tuşuna basılırsa yazılım başlar.



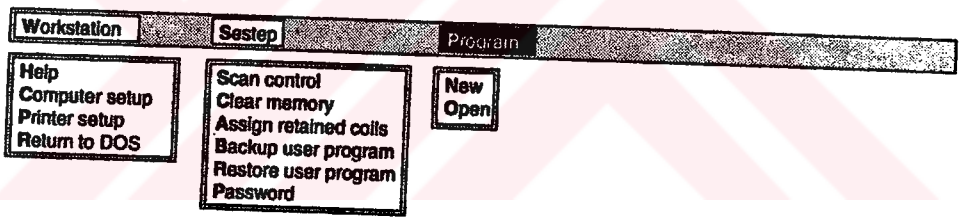
Şekil - 25

3.6 - Menü Yapısı :

PC'deprogramlama kısmı üç menü seviyesine bölünmüştür.

3.6.a - Seviye - 1 - Ana Menü :

Program açıldığında ilk karşımıza gelir. <Sestep>, <Workstaten>, <Program> gelir. Program ile "Path", "Element", "Data" ve "View" menüsü gelir.



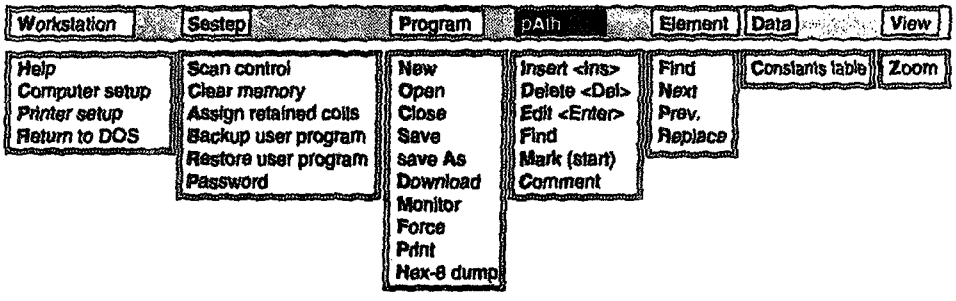
Şekil - 26

3.6.b - Program Menü :

Burada kullanıcı CPU'da yüklenmiş programı değiştire bilir, test edebilir, yazıcı çıkışı alabilir.

Level 2: Program menu

Here the user program can be changed, secured, tested, printed out and loaded in the CPU.



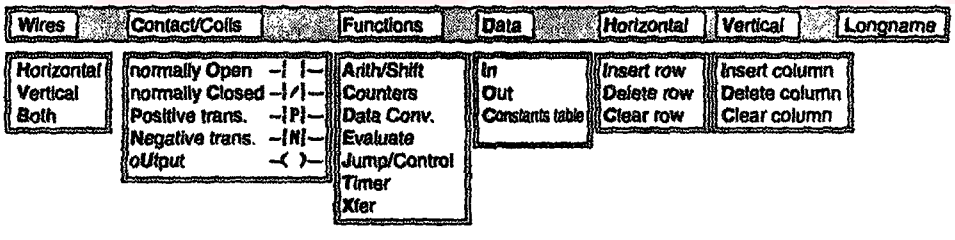
Şekil - 27

3.6.c - Path Menü :

Burada bütün komut ve fonksyonlara ait ihtiyaç olan çizimler bulunur.

Level 3: Path menu

Here all commands and functions are available which are needed for drawing up and changing a path.



Şekil - 28

3.7 : Seviye - 1 Ana Menü

Menü "WORKSTATİON"

Help : <F9> tuşu ve genel kullanım hakkında yardım

Computer Setup : Monitör tipi, bağlantı portu gibi bilgiler ayarlanır.

Printer Setup : Doğru çıkış almak için yazıcı seçimi yapılır.

Return To Dos : PRS - 21'den çıkmamızı sağlar.

Menü "SESTEP"

Bu menü PLC ile bağlantı yapıldığında seçile bilir.

Scan Control : Çalış/Dur moduna geçiş sağlanır.

Clear Memory : - Kullanıcı programı silinir.

- Veri- Hafıza silinir (Özel kütüklerde silinir.)

- Veri Hafıza ve kullanıcı programı silinmesi

Assign retainet coils

Back up User Program :

Hafıza içeriği (CPU'nun) komutları olmadan hard disk'e binary olarak kaydedilir. Ad,<LDD> olarak kaydedilir. (Program - Open -F8)

Restur User Program : CPU'ya binary yüklenen program kopyası.

Password : İstenmeyen kullanmalara karşı koruma.

Menü "Program"

New : Kullanıcı tarafından yeni program oluşturur.

Open : Bulunan programı açmak için kullanılır.

Close : Kullanıcı programı terketmek.

Save : Kullanıcı proramı Hard-Disk'e kopyalar

Save As : Kullanılan bir programı Hard - Disk'yeni adla yüklemekte kullanılır.

Down Load : Kullanıcı programının CPU'ya yüklenmesi

Monitör : Çalıştırılan programda 1-Elemanların durumu (Giriş, çıkış, özel kütükler), 2- Değişkenlerinin içeriklerinin gösterilmesi için kullanılır.

Force : Bu komutla program çalışırken değişkenlerin içerikleri değiştirilir.

Print : (Ad.LST) Olarak yüklenmiş dosyanın LPT 1 üzerinden yazıcıda yazılm ası sağlanır.

Hex-8Dump : EPROM'a yazmak için "Intel Intelex 8 Hexadecimal" formatında PRS - 21 için dosya oluşur.

3.8 - LEVEL 2 : PROGRAM MENÜ :

Menü "Path"

Insert <Ins> : Yenibir yol eklenmesini sağlar.

Delete <Del> : Aktif yol silinir

Edıt <Enter> : Aktif yol değiştirilir.

Find : Belirlenen yola gidilir.

Mark <Start/End> : Bir veya birçok yol işaretlenerek kopyalama, kaydırma ve silme işlemi için işaretlenir.

Comment :

Menü "Element"

Find : Aktif yol ile son yol arasında özel bir elemanı bulur.

Next : Find komutu ile bulunan elemandan sonrakine gitmek için kullanılır.

Prev : Find komutu ile bir önceki değişkene hareket etmek için kullanılır.

Replace : Bir değişkenin başka bir değişkenle değiştirilmesi için kullanılır.

Menü "Data"

Constant table : Komut tablosunda yeni değer girildiğini göstermek için kullanılır.

Menü "View"

Zoom : Bu komutla böyük ve normal görünümde çalışılır. Uzun isimli görünmeyenler, büyütmede modu ile görülür.

3.9 - LEVEL. 3 : Path Menü

Menü "Wires" :

Herizantal : Yatay bağlantı yapılır.

Vertical : Çizgilere dikey bağlantı yapılır.

Both : Yola yatay - dikey bağlantı yapılır.

Menü "Contacts/Coils" (Kontaklar/Sargılar)

Normally Open : Normalde açık kontak yerleştirilir.

Normally Closed : Normalde kapalı kontak yerleştirilir.

Pocitive Trans : Pozitif kenarda çalışan eleman yerleşir.

Negative Trans : Negatif kenarda konum değiştiren eleman yerleşir. Bir program taraması boyunca durum değiştirmez.

Out Put : Çıkış Sargısı yerleşir.

Menü "Functions"

Aritmetik, shift - register, sayıcı ve zamanlayıcı komutları bu program kontrolü içindedir.

Sub - Menü	Fonksiyonlar
Arit/Shift	ADD DIV MUL SHFR SUB
Sayıcı	CNT U/PC
Veri değiştirme	BCD BIN SWAP
Karşılaştırma	CMP
Sıçrama/Kontrol	END ENDS JCR JCS MCS MCR SKIP
Zamanlayıcı	TMR
X fer	XFER

Menü "Data"

In (Giriş) :Elemana girişle aktarma yapılır.

Out (Çıkış) : Elemana çıkışla aktarma yapılır

Constant Table :WC001...WC0512'deki değer kütüklerine giriş yapılır.

Menü "Horizantal"

Incert Row : Boş yatay giriş için aktif olunur.

Delete Row : Aktif olan silinir.

Clear Row : Aktif olan yatay satır silinir.

Menü "Vertical"

Incert Column : Boş kolon girilir.

Delete Colomn : Aktif kolon silinir.

Clear Colomn : Aktif olan dikey kolon silinir.

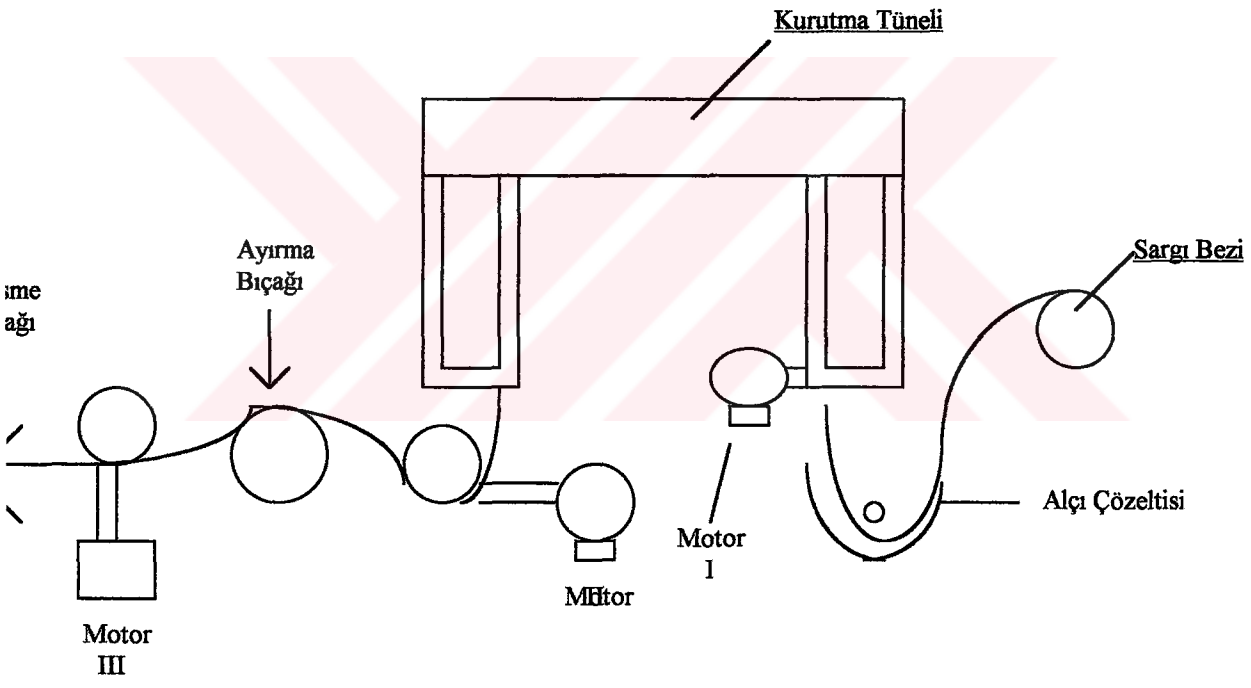
Menü "Long Name"

Elemanlara 21 karakterlik isim verilir. 3 satır - 7 karakter.

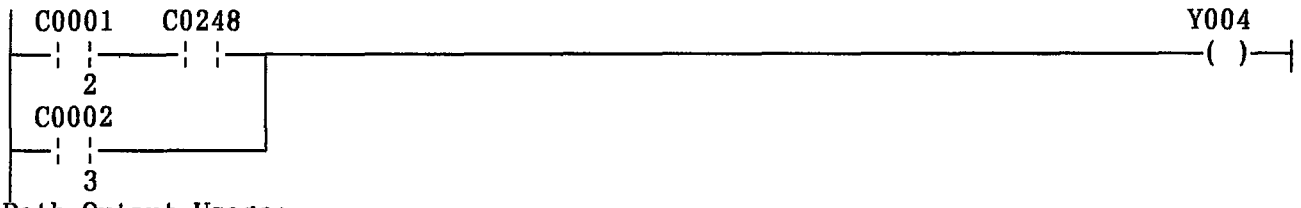
BÖLÜM -4

SESTEP - 190 ile gerçekleştirilen uygulama alçı bezlerinin otomasyonunu gerçekleştirmek üzere düşünülmüştür.

Aşağıda imalat akış resminde görüldüğü üzere, 1,5mt. enindeki sargıbezi topu, alçı çözeltisinden (metilen klorit, methenal, alçı vb.) geçirildikten sonra kurutma tüneline girer. Kurutma tünelinin çıkışında ön kesme bıçaklarından 15cm. aralıklarla kesilerek şeritlere ayrılır. Bu şeritler 2mt. boyunbda kesilerek (Manyetik sensör ve sayıcı aracılığıyla) ambalajlama bölümüne sevk edilecek hale gelir.

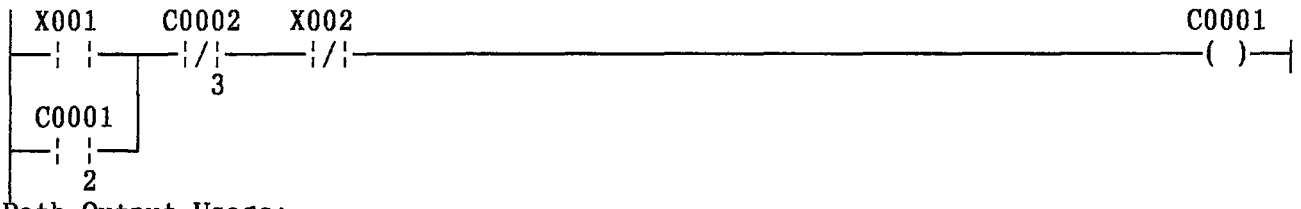


1 . Path



Path Output Usage:
Y004 (not used in any other path)

2 . Path

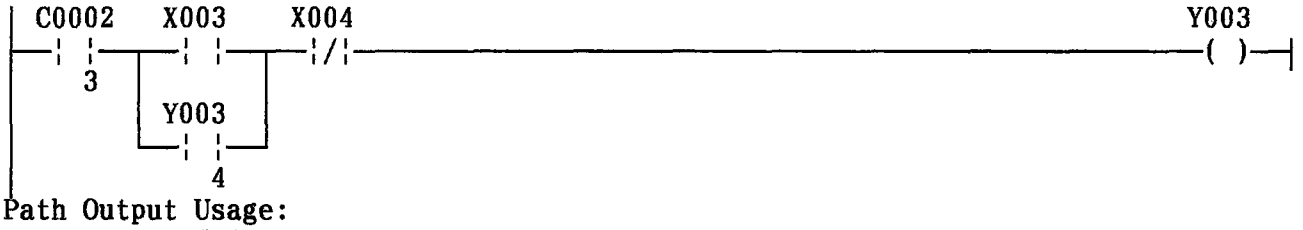


Path Output Usage:
C0001 (used in) 1,2,3

3 . Path

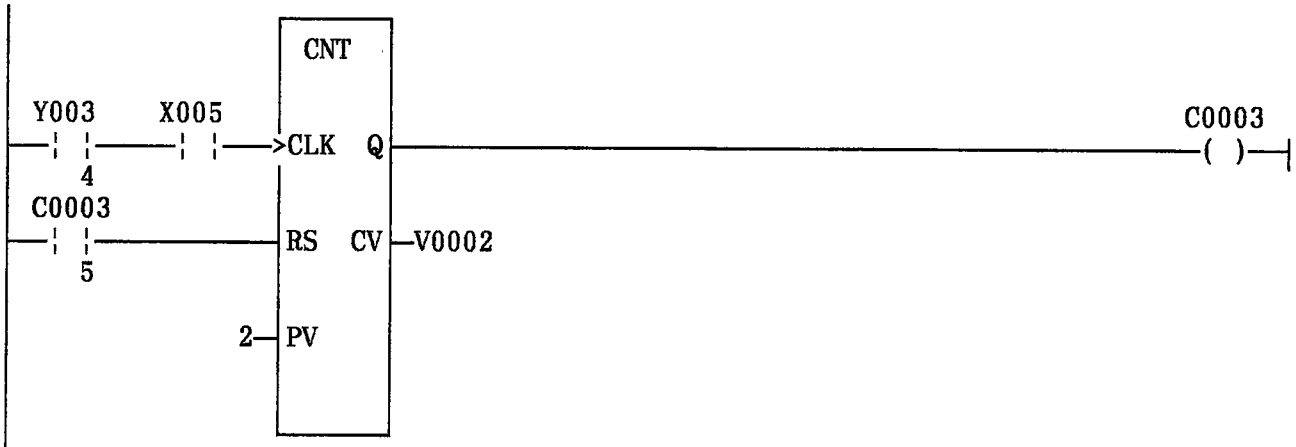
Path Output Usage:
C0002 (used in) 1,/2,4
V0001 (not used in any other path)

4 . Path



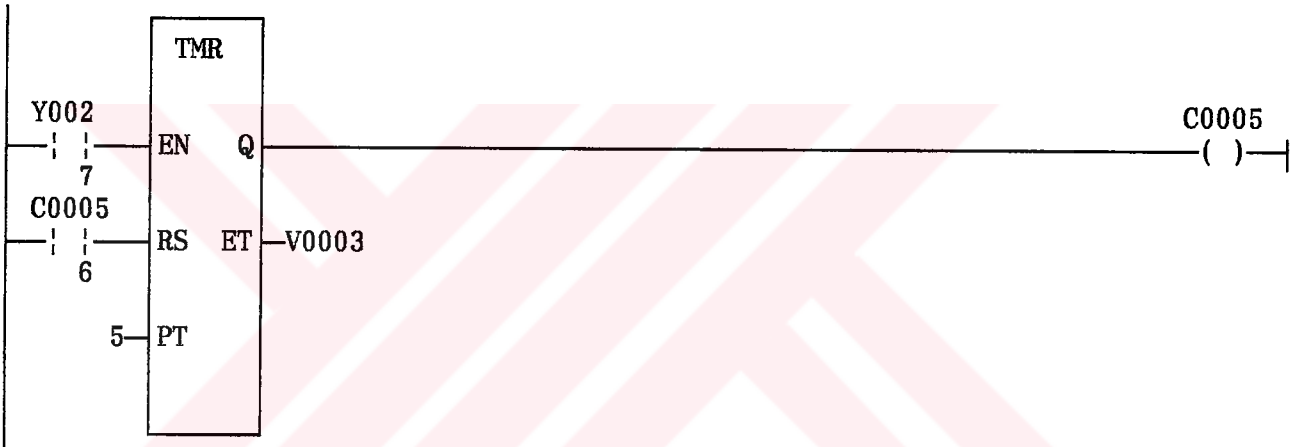
Path Output Usage:
Y003 (used in) 4,5,7,8

5 . Path



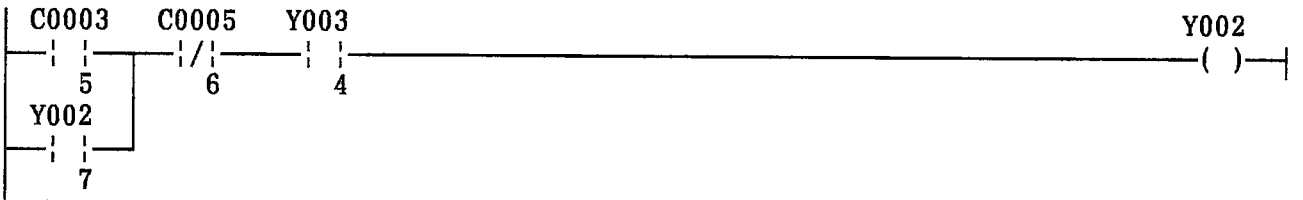
Path Output Usage:
C0003 (used in) 5,7
V0002 (not used in any other path)

6 . Path



Path Output Usage:
C0005 (used in) 6,/7
V0003 (not used in any other path)

7 . Path



Path Output Usage:
Y002 (used in) 6,7

8 . Path

Path Output Usage:
Y001 (not used in any other path)

Element	Description	Source	Used in
C0001		2	1,2,3
C0002		3	1,/2,4
C0003		5	5,7
C0005		6	6,/7
C0248			1
V0001		3	
V0002		5	
V0003		6	
X001			2
X002			/2,3
X003			4
X004			/4
X005			5,8
Y001		8	
Y002		7	6,7
Y003		4	4,5,7,8
Y004		1	

Contents Chapter 3

Introduction

A control task is managed by creating a user program. The input signals are logically linked with internal registers, timing elements and counters, depending on the specifications of the task. The results of these operations set the appropriate outputs.
Using the programming software on a PC, programs can be written in Ladder Diagram, using the hand programming device in Instruction List. Within the control device the user program is converted into a common machine code, which can be decompiled back to either method of representation. Within the programming software the program can be displayed as Ladder Diagram and as Instruction List but on the hand programming device exclusively as Instruction List.

Ladder Diagram (LD)

In principle, the Ladder Diagram is a way of converting an electrical circuit diagram into graphical program with elements like normally-open contacts, normally-closed contacts, wiper contacts and coils. The instruction set is augmented by such functions as timing elements, counters and function blocks. Ladder Diagram provides a clear graphic display of linkages. The language elements are arranged horizontally, and the complete paths one beneath another. The address of each language element is shown immediately above it.

Instruction List (IL)

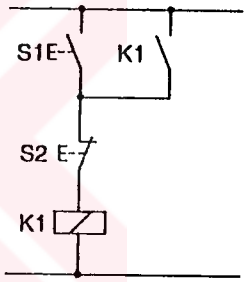
An instruction list is derived from the electrical diagram, and this is converted into the mnemonic abbreviations of the instruction set. Each mnemonic abbreviation corresponds to a particular graphical symbol in Ladder Diagram. This makes Instruction List and Ladder Diagram compatible. In the Instruction List format, the language elements are written one beneath another. The address of each language element is shown to the right of it, on the same line.

On execution of the program, one instruction after another is executed. The inputs X retain their status during one complete program scan. The internal registers C, the outputs Y and the contents of the registers are constantly updated during the program scan. But the physical outputs are set on or off only after termination of the scan according to the corresponding status.

Programming for Safety

Just as much attention must be given to safety aspects in programming a PLC as when conventional control technology is being used. Signals from switches which have personnel protection functions, such as an EMERGENCY STOP, should never be routed through a PLC. These switches must provide a direct break in the power circuit concerned.
On safety grounds, inputs should be tested for the logical value 1. In the example below of a hold-on mechanism, it will become evident why this is important.

Circuit diagram

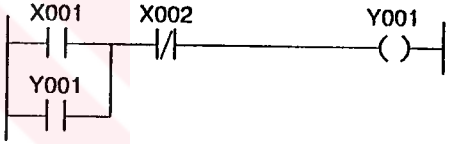


Description of the circuit
Using conventional technology, the off switch (S2) would be a normally-closed switch. Among other consequences, this would ensure that, in the event of a breakage in the wiring for the off switch (S2), the contactor would trip.

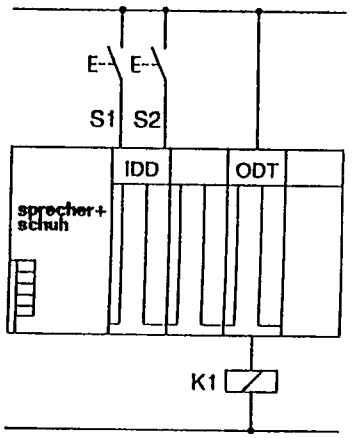
Two solutions are shown how the hold-on circuit could be translated into a Ladder Diagram. Both solutions are functionally correct, but the first is wrong on grounds of safety considerations.

a.) Incorrect solution on safety grounds:

Ladder Diagram



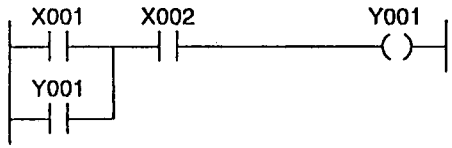
External wiring



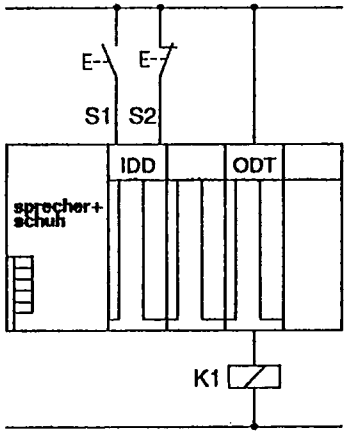
The Ladder Diagram has been copied directly from the circuit diagram. As long as there is no fault during operation, this circuit will perform its function perfectly adequately, except that in order to switch off the contactor, the off switch (S2) must be switched on. The result of this is that if there is a breakage in the wiring of the off switch (S2), it will be impossible to break the hold-on which holds the contactor on.

b.) Correct solution on safety grounds:

Ladder Diagram



External wiring



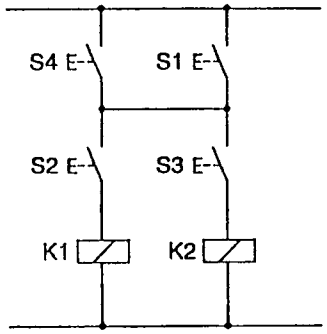
The off switch (S2) is tested for logical **1**. At first sight this may seem contradictory. However, the external wiring must also be taken into account. The off switch (S2) is wired as normally-closed contact, so that the input X2 will normally be at the high potential.
When the off switch (S2) is pressed, i.e. the circuit is broken, the hold will be broken. This also ensures that if there is a break in the wiring to the off switch (S2), the contactor will cut out.

Notes on Programming

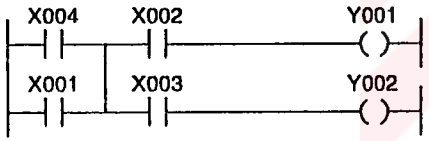
There are fundamental differences between relay circuits and those to be executed on a PLC. It is not always possible to copy the Ladder Diagram representation of the user program directly off the circuit diagram.
The following example shows the points which have to be taken into account in translating a circuit diagram into a Ladder Diagram.

Example

Circuit diagram:



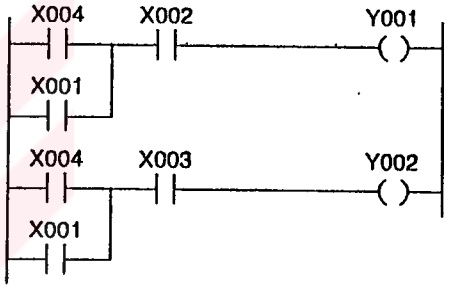
Wrong solution:



The direct translation of the circuit diagram into Ladder Diagram is not programmable.

The following section shows two possible correct ways of deriving a Ladder Diagram from the circuit diagram.

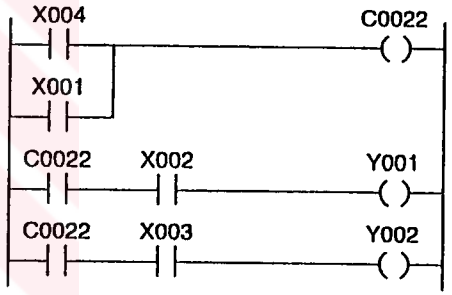
Solution 1:



STR	X004
OR	X001
AND	X002
OUT	Y001
STR	X004
OR	X001
AND	X003
OUT	Y002

Solution 2:

Ladder Diagram using the internal register C0022.



STR	X004
OR	X001
OUT	C0022
STR	C0022
AND	X002
OUT	Y001
STR	C0022
AND	X003
OUT	Y002

Description of the Data Memory

Elements	SESTEP 190 / 290 PCU-21 No.	Range	SESTEP 290 PCU-20 No.	Range
Inputs	128	X001...X128	128	X001...X128
Outputs	128	Y001...Y128	128	Y001...Y128
Internal registers	992	C0001...C0232 C0265...C1024	232	C0001...C0232
Special internal registers	32	C0233...C0264	24	C0233...C0256
Constant registers	512	WC001..WC512		
Counters / timers	64 4	V0001...V0064 V0157...V0160	64	V0001...V0064
High-speed counter	1	V0065	1	V0065
Registers	831	V0066...V0128 V0257...V1024	63	V0066...V0128
Special registers	128	V0129...V0256	16	V0129...V0144
Input registers	16	WX01...WX16	16	WX01...WX16
Output registers	16	WY01...WY16	16	WY01...WY16
Sequencers	8	S101...S116 : : S801...S816	8	S101...S116 : : S801...S816

- Input/output registers are used as auxiliary registers.
- Inputs/outputs which are not assigned to a module may be used as internal registers.
- Counters and timers may be used as auxiliary registers.
- V, WX and WY are 16 bit registers.

Status after a power failure or when the CPU is in STOP mode:

Outputs, internal registers	can be defined as non-volatile
Special internal registers, constant registers	non-volatile
Counters/timers	will be reset, if C0238 = OFF will be retained, if C0238 = ON
Registers, input registers, output registers, high-speed counter	will be reset, if C0240 = OFF will be retained, if C0240 = ON
Special registers	depends on the function
Sequencers	depend on the contents of the registers V0001...V0008

Functions of the Special Internal Registers

The following special internal registers can be set or reset by the user. Their coils and contacts can also be utilised in the application program.

C0233 When C0233 is set active, all outputs are forced to OFF.

C0234 When C0234 is active/inactive, the high-speed counter is started/stopped.

C0235 When C0235 is active, the content of the register V0065 (high-speed counter) is cleared.

C0236 This internal register can be forced ON/OFF by use of the programming device. When it is set ON, all outputs and internal registers can be used several times as a coil.

C0237 This internal register can be forced ON/OFF by use of the programming device. If it is set ON whilst the processor is inactive, all forced inputs/outputs and internal registers, with the exception of the special internal registers, will be set OFF. C0237 is automatically reset to OFF.

C0238 This internal register can be forced ON/OFF by use of the programming device. If it is set ON, the counter/timer elements (V0001...V0064) will be retained when the device is switched OFF.

C0239 This internal register can be forced ON/OFF by use of the programming device. If it is set OFF, the state of the outputs will be maintained whilst the CPU is in STOP mode. Otherwise the outputs will be set inactive.

C0240 This internal register can be forced ON/OFF by use of the programming device. If it is set ON, the contents of all registers will be retained if there is a power failure or if the CPU is in STOP mode.

The user can neither set nor reset the following special internal registers. However, their contacts can be utilised in the application program.

C0241 No carry bit - NC (non carry)

C0242 Carry bit - C (carry)

C0243 Zero bit - Z (zero)

C0244 Error bit - ERR (error)

C0245 Ever off - special internal register is always OFF

C0246 0,1 second cycle time

C0247 0,4 second cycle time

C0248 0,8 second cycle time

C0249 If this special internal register is ON, this indicates a memory error.

C0250 If this special internal register is ON, this signals that the preceding Process Reset has not been correctly executed.

C0251 If this special internal register is ON, it indicates a defect input or output module.

C0252 Reserved

High-speed Counter

The SESTEP 190 and the SESTEP 290 are equipped with a high-speed counter.

High-speed Counter of the SESTEP 190

Input X001 is used as the counter input. A 2 phase counter is available in some basic units, in which case input X002 is used as second phase.

Technical data

Inputs

Counter input	X001
Input for second phase	X002 (option)
Input voltage	24 VDC
Control voltage for ON	9...28 VDC
Control voltage for OFF	0...5 VDC
Signal form	rectangular, sine
Pulse width	min. 60 µs
Frequency	max. 8 kHz (5 kHz for 2 phase counter)

Registers

Counter register	V0065 range: 0...65535 (16 bits)
Preset register	V0161 range: 0...65535 (16 bits)

Internal registers

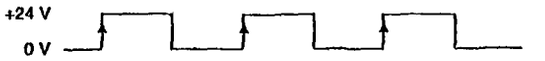
C0234	enable	ON = counter enabled OFF = counter disabled
C0235	reset	ON = counter reset, V0065 = 0, C0264 = OFF
C0261	counter selection	OFF = single-phase counter ON = 2 phase counter (option)
C0262	counter direction	OFF = incremental counter ON = decremental counter

C0264 comparator signal	counter direction:	increment C0262 = OFF	decrement C0262 = ON
	V0065 > V0161	ON	OFF
	V0065 < V0161	OFF	ON
	V0065 = V0161	ON	ON

Single-phase counter

Incremental counter

C0261 = OFF, C0262 = OFF



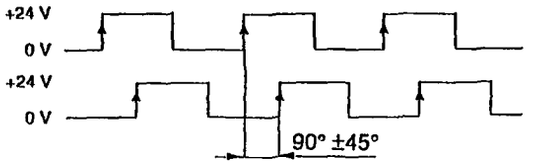
Decremental counter

C0261 = OFF, C0262 = ON

2 phase counter (option)

Incremental counter

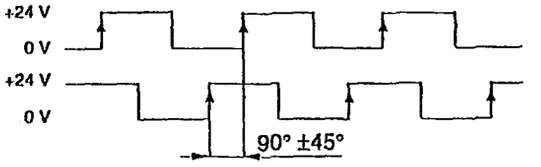
C0261 = ON, C0262 = inactive



The content of the counter register is increased by one, if the edge at input X002 in relation to the edge at input X001 is behind by 90°.

Decremental counter

C0261 = ON, C0262 = inactive



The content of the counter register is decreased by one, if the edge at input X002 in relation to the edge at input X001 is in front by 90°.

(programming example, see page 3.83)

High-speed Counter of the SESTEP 290

The counter input is integrated into the terminal (HS CTR) of the CPU module.

Technical data

Input

Counter input	terminal HS CTR on the CPU module
Input voltage	24 VDC
Voltage range	10.8...26.4 VDC
Control voltage for ON	min. 10.8 VDC, min. 6 mA
Control voltage for OFF	max. 2 VDC, max. 0.5 mA
Signal form	rectangular, sine
Pulse width	min. 80 µs
Frequency	max. 5 kHz

Registers

Counter register	V0065 range: 0...65535 (16 bits)
Preset register	V0161 range: 0...65535 (16 bits) (only PCU-21)

Internal registers

C0234 enable	ON = counter enabled OFF = counter disabled
C0235 reset	ON = counter reset, V0065 = 0, C0264 = OFF
C0262* counter direction	OFF = incremental counter ON = decremental counter

C0264* comparator signal

counter direction:	increment C0262 = OFF	decrement C0262 = ON
V0065 > V0161	ON	OFF
V0065 < V0161	OFF	ON
V0065 = V0161	ON	ON

* These special internal registers can only be used with the CPU module PCU-21 of the SESTEP 290.

(programming example, see page 3.86)

Real Time Clock

The SESTEP 190 and the SESTEP 290 (PCU-21) are available with an internal real time clock (option). The time and the date are stored in real time registers and can be written and read through special registers.

Special registers

V0149	Week-day	[1...7]	1 = Monday, 7 = Sunday
V0150	Hour	[0...23]	
V0151	Minute	[0...59]	
V0152	Second	[0...59]	
V0153	Year	[0...99]	
V0154	Month	[1...12]	
V0155	Day	[1...31]	

Special internal register

C0263 Write protection flag

Register = OFF: The special registers of the clock are write protected. In the RUN mode the special registers are continously refreshed with the values of the real time registers.

Register = ON: The special registers of the clock can be written.
At the negative edge of C0263 the values, which are in the special registers, are transferred to the real time registers.

30 s adjustment At the positive edge of the internal register C0263, the second register V0152 is set to 0, if the content was between 0...29. If the content was between 30...59 the register V0152 is set to 0 and the minute register V0151 is incremented by 1.

Steps for adjusting the clock

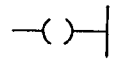
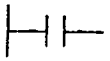
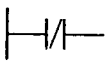
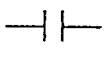
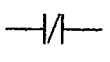
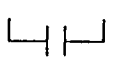
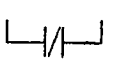
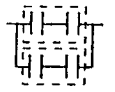
- Switch on C0263.
- Write time, date and week-day into the corresponding special registers.
- Switch off C0263.

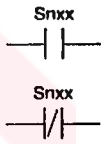
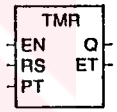
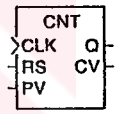
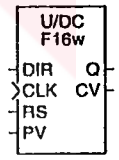
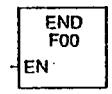
Lifetime of the battery

S190	10 years
S290 (PCU-21)	5 years

(programming example, see page 3.87)

Summary of the Instructions

Ladder Diagram	Instruction List	Instruction Name	Function	See page
	OUT	Output	Assign the result of a logic operation to an output of type Y or C.	3.22
	STR	Store	Start a logic operation with a normally-open contact of type X, Y, C or S.	3.23
	STR NOT	Store Not	Start a logic operation with a normally-closed contact of type X, Y, C or S.	3.23
	AND	And	Sequential link of a logic operation with a normally-open contact of type X, Y, C or S.	3.24
	AND NOT	And Not	Sequential link of a logic operation with a normally-closed contact of type X, Y, C or S.	3.24
	OR	Or	Parallel link of a logic operation with a normally-open contact of type X, Y, C or S.	3.25
	OR NOT	Or Not	Parallel link of a logic operation with a normally-closed contact of type X, Y, C or S.	3.25
	AND STR	And Store	Sequential link of two blocks of parallel links with elements of type X, Y, C or S.	3.26
	OR STR	Or Store	Parallel link of two blocks of sequential links with elements of type X, Y, C or S.	3.27

Ladder Diagram	Instruction List	Instruction Name	Function	See page
	F-05_DIFO	Positive edge detection	Sequential link of a positive edge detection. A change in the signal from OFF to ON will be recognised, and the contact will remain set ON for one program cycle.	3.28
	F-06_DIFF	Negative edge detection	Sequential link of a negative edge detection. A change in the signal from ON to OFF will be recognised, and the contact will remain set ON for one program cycle.	3.29
	V000n	Sequencer	A sequencer is set up using registers V1...V8 and contacts of normally-open or normally-closed type designated as S. The reference number of the V register corresponds to the 1st number in the contact definition. The content of this register shows which of the steps 1...16 is being addressed.	3.30
	TMR ET PT	Switch-on time delay element	As long as the input EN=ON, the timing element will count in 100 ms steps, until the set value is reached. **RS = ON → ET = 0**	3.32
	CNT CV PV	Incremental counter	The incremental counter adds 1 to the value in the current value register **CV** every time that a positive edge is applied to the input **CLK**. **RS = ON → CV = 0**	3.33
	F-16_CNT CV PV	16 bit incremental/ decremental counter	As long as the input DIR=ON, the counter starts from the value held in register **PV** and counts upwards, putting the result in register **CV**. At DIR=OFF the counter counts downwards. **RS = ON → CV = 0**	3.34
	F-00_END	End of program	The F-00 instruction marks the end of program. It results in a jump back to the address 0. The F-00 instruction may not be subject to any control condition.	3.36

Ladder Diagram	Instruction List	Instruction Name	Function	See page
MCS F01 EN	F-01_MCS	Main circuit start	The F-01 instruction marks the start of the main functional circuit. If the control condition EN=ON, the instructions between F-01 (MCS) and F-02 (MCR) will be executed. If the control condition EN=OFF, the instructions between F-01 (MCS) and F-02 (MCR) will not be executed, programmed outputs and internal registers will be switched off.	3.37
MCR F02 EN	F-02_MCR	Main circuit return	The F-02 instruction marks the end of the main circuit. The F-02 instruction may not be subject to any control condition.	3.37
JCS F03 EN	F-03_JCS	Jump circuit start	The F-03 instruction marks the start of an instruction jump. If the control condition EN=ON, the instructions between F-03 (JCS) and F-04 (JCR) will be regarded as NOP. The contents of the registers and the state of any outputs which are skipped will be maintained.	3.39
JCR F04 EN	F-04_JCR	Jump circuit return	The F-04 instruction marks the end of a block of instructions to be skipped. The F-04 instruction may not be subject to any control condition.	3.39
SKIP F07 EN	F-07_SKIP	Start of SKIP	If the control condition EN=ON, the instructions between F-07(SKIP) and F-08 (ENDS) will be skipped over. The F-07 (SKIP) instruction effects a reduction in the execution time.	3.44
ENDS F08 EN	F-08_ENDS	End of SKIP	The F-08 instruction marks the end of the section to be skipped. The F-08 instruction may not be subject to any control condition.	3.44

Ladder Diagram	Instruction List	Instruction Name	Function	See page
SWAP F09w TR REG	F-09w SWAP REG	16 bit swap	The content of L byte in register **REG** will be swapped with the content of H byte in register **REG**.	3.47
SHFR F10w DIR IN CLK RST REG	F-10w SFR REG	16 bit registers shift, bi-directional	A positive edge at the input **CLK** will cause the content of register **REG** to be shifted one place. The carry will be stored in the carry bit register. **RST = ON → REG = 0**	3.48
XFER F11 EN FRM TO	F-11_XFER TO FRM	8 bit transfer	The content of register **FRM** (L byte) will be copied into register **TO** (L byte).	3.50
XFER F11w EN FRM TO	F-11w XFER TO FRM	16 bit transfer	The content of register **FRM** will be copied into register **TO**.	3.52
BCD F12 EN B BCD	F-12_BCD BCD B	8 bit binary to BCD	The content of register **B** (L byte) will be converted to a BCD number and stored in register **BCD** (L byte).	3.54
BCD F12w EN B BCD	F-12w BCD BCD B	16 bit binary to BCD	The content of register **B** will be converted to a BCD number and stored in register **BCD**.	3.56
ADD F13 EN IN TO	F-13_ADD TO IN	8 bit addition	The content of register **TO** (L byte) will be added to the content of register **IN** (L byte). The result will be stored in register **TO+1** (L byte). **TO+1 = IN+TO**	3.58
ADD F13w EN IN TO	F-13w ADD TO IN	16 bit addition	The content of register **TO** will be added to the content of register **IN**. The result will be stored in register **TO+1**. **TO+1 = IN+TO**	3.60

Ladder Diagram	Instruction List	Instruction Name	Function	See page
SUB F14 EN FR SB↓	F-14_SUB SB FR	8 bit subtraction	The content of register **SB** (L byte) will be subtracted from the content of register **FR** (L byte). The result will be stored in register **SB+1** (L byte). **SB+1 = FR-SB**	3.62
SUB F14w EN FR SB↓	F-14w SUB SB FR	16 bit subtraction	The content of register **SB** will be subtracted from the content of register **FR**. The result will be stored in register **SB+1**. **SB+1 = FR-SB**	3.64
CMP F15 EN IN TO	F-15_CMP TO IN	8 bit comparison	The content of register **IN** (L byte) will be compared with the content of register **TO** (L byte) to see if it is =, < or >.	3.66
CMP F15w EN IN TO	F-15w CMP TO IN	16 bit comparison	The content of register **IN** will be compared with the content of register **TO** to see if it is =, < or >.	3.68
BIN F17 EN BCD B	F-17_BIN B BCD	8 bit BCD to binary	The BCD number of register **BCD** (L byte) will be converted to a binary number and stored in register **B** (L byte).	3.70
BIN F17w EN BCD B	F-17w BIN B BCD	16 bit BCD to binary	The BCD number of register **BCD** will be converted to a binary number and stored in register **B**.	3.72
MUL F18w EN MR MN↓	F-18w MUL MN MR	Multi-plication	The content of register **MR** will be multiplied by the content of register **MN** and the result stored in the registers **MN+2** and **MN+1**. **MN+2, MN+1 = MRxMN**	3.74
DIV F19w EN DR DN↓	F-19w DIV DN DR	Division	The content of registers **DN+1, DN** will be divided by the content of register **DR** and the result stored in the registers **DN+3** and **DN+2**. **DN+3, DN+2 = DN+1, DN/DR**	3.76

Description of the Instructions

A uniform presentation has been adopted for describing the individual instructions in detail. The following is a key to the various parts of each definition:

1. Heading block

The heading block contains the main parameters for each instruction, displayed so that they can be seen at a glance:

Instruction name		Trigg. cond.	No. of steps	Execution time µs	Input programming device
Instruction IL	Instruction LD	EN 1	1	active max. 13 inactive max. 9	OUT Operand ENTER

Abbreviations for "control conditions":
0 = Signal OFF
1 = Signal ON
↑ = Swap from OFF to ON
↓ = Swap from ON to OFF
x = No change

Note for "number of program steps":
If the internal registers C0256...C1024 are used in the instructions OUT, STR, STR NOT, AND, AND NOT, OR and OR NOT, they need 2 program steps.

2. Function

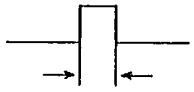
The instruction is explained.
For functions the allowed ranges of the used elements are listed.

Note:
The upper limits for internal registers and registers are valid only for the SESTEP 190 and the CPU module PCU-21 of the SESTEP 290. The CPU module PCU-20 of the SESTEP 290 has smaller ranges, which are listed in the table of the data memory on page 3.6.

3. Programming example

A short programming example is shown for Ladder Diagram (PRS-21) and for Instruction List (PRG-20/21).

Note:
A signal, which has exactly the length of 1 program cycle, is shown the following way:

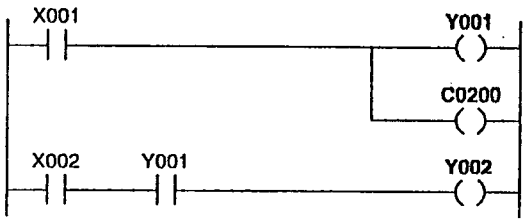


Output		Trigg. cond.	No. of steps	Execution time µs	Input programming device
OUT	—( )—	1	1	active max. 13 inactive max. 9	OUT Operand ENTER

Function
Assigns the result of a logic operation to an output of type Y (physical outputs) or type C (internal outputs, internal registers). If the signal applied is logical 1, the output will switch ON.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X001
OUT	**Y001**
OUT	**C0200**
STR	X002
AND	C0200
OUT	**Y002**

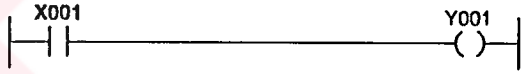
The output Y001 and the internal register C0200 will be switched on if the contact X001 is closed. The output Y002 will be switched on if both X001 and X002 are closed. Outputs and internal registers may be used in parallel exactly as required.

Store		Trigg. cond.	No. of steps	Execution time µs	Input programming device
STR	—| |—		1	active max. 6 inactive max. 6	STR Operand ENTER

Function
Start a logical operation with a normally-open contact of type X, Y, C or S.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	**X001**
OUT	Y001

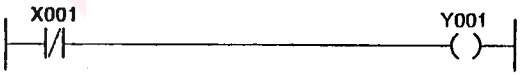
The output Y001 will be switched on if the normally-open contact X001 is closed. As soon as the normally-open contact X001 is opened, the output Y001 will switch off.

Store Not		Trigg. cond.	No. of steps	Execution time µs	Input programming device
STR NOT	—|/|—		1	active max. 6 inactive max. 6	STR NOT Operand ENTER

Function
Start of a logical operation with a normally-closed contact of type X, Y,C or S.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

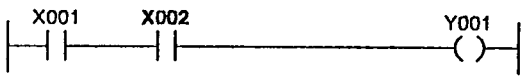
STR NOT	**X001**
OUT	Y001

In its unactuated state, the normally-closed contact X001 will be closed, and the output Y001 will be switched on. As soon as the normally-closed contact X001 is opened, the output Y001 will switch off.

And		Trigg. cond.	No. of steps	Execution time µs	Input programming device
AND	—| |—		1	active max. 6 inactive max. 6	AND Operand ENTER

Function
Sequential link of a logic operation with a normally-open contact of type X, Y, C or S.
A maximum of 8 elements can be linked in series in each circuit.

Programming example
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X001
AND	**X002**
OUT	Y001

The normally-open contact X001 is linked in series with another normally-open contact X002. The output Y001 will switch on if both the normally-open contacts are closed. As soon as either of the normally-open contacts is opened, the output Y001 will switch off.

And Not		Trigg. cond.	No. of steps	Execution time µs	Input programming device
AND NOT	—|/|—		1	active max. 6 inactive max. 6	AND NOT Operand ENTER

Function
Sequential link of a logic operation with normally-closed contact of type X, Y, C or S.
A maximum of 8 elements can be linked in series in each circuit.

Programming example
Ladder Diagram
Programming software PRS-21:

Instruction List
Programming device PRG-20/21:

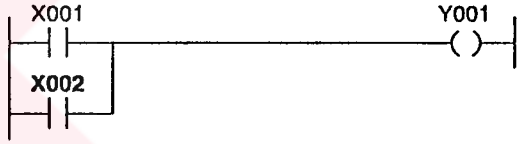
STR	X001
AND NOT	**X002**
OUT	Y001

The normally-open contact X001 is linked in series with the normally-closed contact X002. The output Y001 will be switched on if the normally-open contact X001 and the normally-closed contact X002 are closed. As soon as either of the contacts is opened, the output Y001 will switch off.

Or		Trigg. cond.	No. of steps	Execution time µs	Input programming device
OR	└| |┘		1	active max. 6 inactive max. 6	OR Operand ENTER

Function
Parallel link of a logical operation with a normally-open contact of type X, Y, C or S.
A maximum of 9 elements can be linked in parallel in each circuit.

Programming example
Ladder Diagram PRS-21:



Instruction List PRG-20/21:

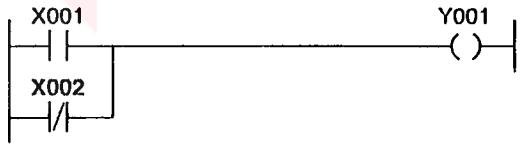
STR	X001
OR	**X002**
OUT	Y001

The normally-open contacts X001 and X002 are linked in parallel. The output Y001 will be switched on as soon as one of the normally-open contacts X001 or X002 is closed. As soon as either of the two contacts is closed, the output Y001 will switch off.

Or Not		Trigg. cond.	No. of steps	Execution time µs	Input programming device
OR NOT	└|/|┘		1	active max. 6 inactive max. 6	OR NOT Operand ENTER

Function
Parallel link of a logical operation with a normally-closed contact of type X, Y, C or S.
A maximum of 9 elements can be linked in parallel in each circuit.

Programming example
Ladder Diagram PRS-21:



Instruction List PRG-20/21:

STR	X001
OR NOT	**X002**
OUT	Y001

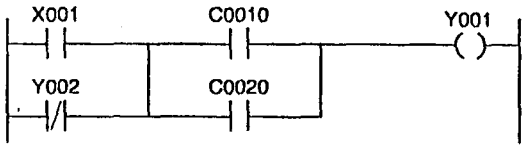
The normally-open contact X001 is combined logically in parallel with the normally-closed contact X002. The output Y001 will be switched on when either contact X001 or contact X002 is closed. As soon as neither of the two contacts is closed, the output Y001 will switch off.

And Store		Trigg. cond.	No. of steps	Execution time µs	Input programming device
AND STR			1	active max. 4 inactive max. 4	AND STR ENTER

Function
Sequential link of two blocks of linked elements of types X, Y, C or S.
This instruction is a logic operation and not a contact operation.

Programming example

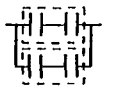
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X001
OR NOT	Y002
STR	C0010
OR	C0020
AND STR	
OUT	Y001

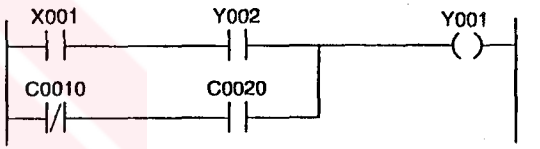
The block which contains the contacts X001 and Y002 linked in parallel is then linked in series with another block containing the contacts C0010 and C0020 which are linked in parallel. The output Y001 will be switched on when either the normally-open contact X001 or the normally-closed contact Y002 is closed, and at the same time either of the normally-open contacts C0010 or C0020 is closed. As soon as both contacts within one of the two blocks are open, the output Y001 will switch off.

Or Store		Trigg. cond.	No. of steps	Execution time µs	Input programming device
OR STR			1	active max. 4 inactive max. 4	OR STR ENTER

Function
Parallel link of two blocks of logically combined elements of types X, Y, C or S.
This instruction is a logic operation and not a contact operation.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X001
AND	Y002
STR NOT	C0010
AND	C0020
OR STR	
OUT	Y001

The block which contains the contacts X001 and Y002 linked in series is then linked in parallel with another block containing the contacts C0010 and C0020. The output Y001 will be switched on when either the normally-open contacts X001 and Y002 are both closed, or the normally-closed contact C0010 and the normally-open contact C0020 are closed. As soon as one contact is opened in each of the blocks, the output Y001 will switch off.

Sequencer		Trigg. cond.	No. of steps	Execution time µs	Input programming device
V000n	Snxx			active min. 39 max. 39 inactive min. 35 max. 43	STR OR Operand AND ENTER
	Snxx				STR OR NOT Operand AND ENTER

V000n = Register V0001...V0008
S = Sequencer contact
n = A number from 1...8 corresponding to register V000n
xx = Step 1...16

Function

A sequencer is specified by one of the registers V0001...V0008, and normally-open or normally-closed contacts designated by S.
The reference number of the V register corresponds to the number in the contact definition.
The contents of the register indicate which of steps 1...16 is being addressed.
Sequencer contacts can be linked in series or in parallel.

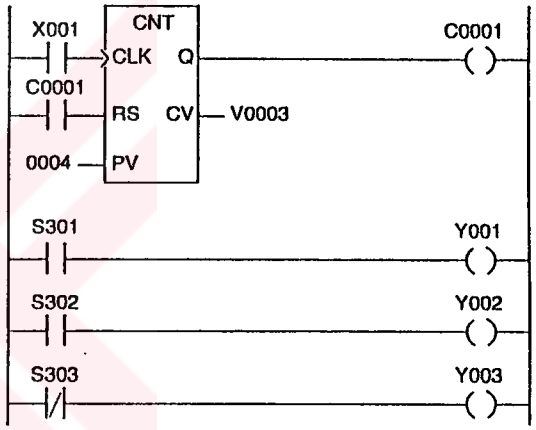
Example

'0001 = 8 --> S108 ON

'0007 = 11 --> S711 ON

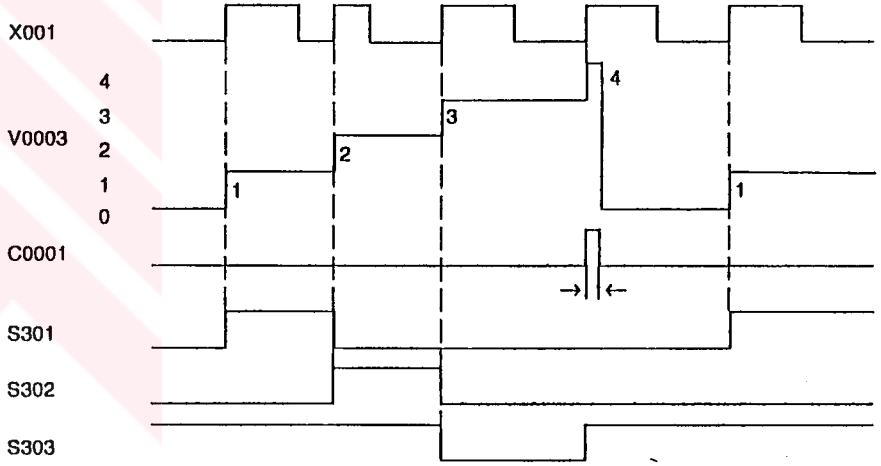
Programming example using a counter

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR      X001
STR      C0001
CNT      V0003  0004
OUT      C0001
STR      S301
OUT      Y001
STR      S302
OUT      Y002
STR NOT  S303
OUT      Y003
```



On-delay timer		Trigg. cond.	No. of steps	Execution time µs	Input programming device
TMR	TMR EN Q RS ET PT	EN 1	2	active max.105 inactive max. 91	TMR Operand (ET) → Operand (PT) ENTER

EN = Start input
RS = Reset input
PT = Set point value register
Q = Output
ET = Current value register

Function

The timer will count up towards the set value, as long as there is a logical 1 signal at the **EN** input, in 100 ms steps or in 10 ms steps. As soon as the value in the **ET** register is equal to or greater than the set value in the **PT** register, the output **Q** will switch on.

Register PT:
Y001, 009, 017...113
X001, 009, 017...113
WY01...16
WX01...16
C0001, 0009, 0017...1009
WC001...WC512
V0001...1024
Constants 0...3999

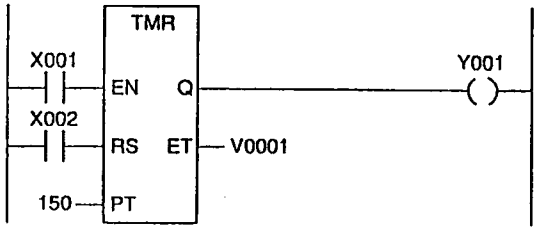
Register ET:
V0001...V0064 (100 ms)
V0157...V0160 (10 ms)

All the variables contained in the registers **PT** and **ET** are in the range 0...65535.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Programming example

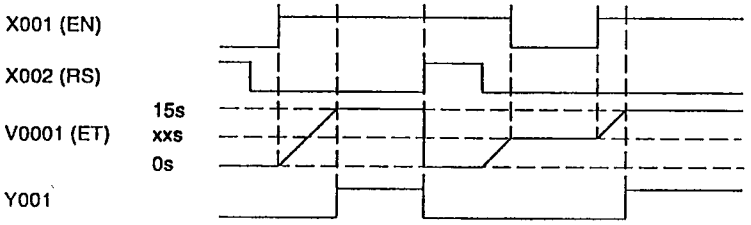
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR   X001
STR   X002
TMR   V0001  0150
OUT   Y001

Set value = 150 (15s)
```



Up counter		Trigg. cond.	No. of steps	Execution time µs	Input programming device
CNT	CNT CLK Q RS CV PV	CLK ↑	2	active max.104 inactive max. 91	CNT Operand (CV) → Operand (PV) ENTER

CLK = Count input
RS = Reset input
PV = Set point value register
Q = Output
CV = Current value register

Function

The counter increments the value by 1 in the current value register **CV** with each positive edge applied to the input **CLK**. If the actual value is equal to or greater than the set value **PV**, the output **Q** will be switched on. Subsequent impulses at the counter input will then be ignored. The current value stays the same as the set value **PV**.

Register PV:
Y001, 009, 017...113
X001, 009, 017...113
WY01...16
WX01...16
C0001, 0009, 0017...1009
WC001...512
V0001...1024
Constants 0...3999

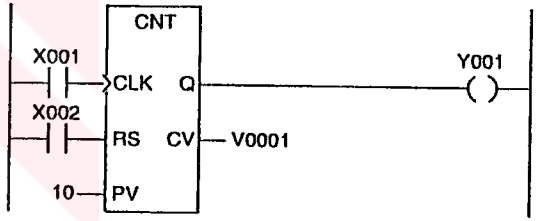
Register CV:
V0001...V0064

All the variables contained in the registers **PV** and **CV** are in the range 0...65535.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Programming example

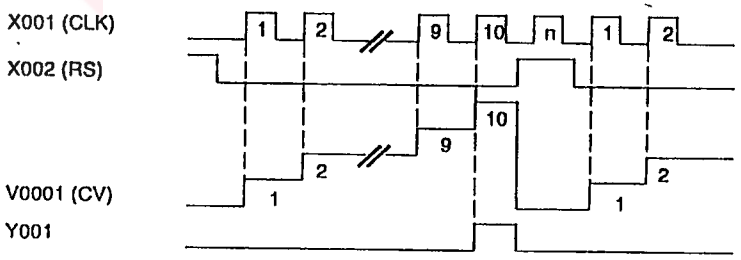
Ladder Diagram PRS-21:



Instruction List PRG-20/21:

```
STR   X001
STR   X002
CNT   V0001  0010
OUT   Y001

(Set value = 10)
```



16 bit up/down counter		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-16_CNT	U/DC F16w DIR Q CLK CV RS PV	CLK ↑	3	active min. 108 max.118 inactive min. 103 max.103	FUN 1 6 → Operand CV → Operand PV ENTER

DIR = Count direction
CLK = Count input
RS = Reset input
PV = Set point value register
Q = Output
CV = Current value register

Function

The counter counts incrementally in register **CV** up to a value in register **PV**, or decrementally in register **CV** starting with a value taken from register **PV**. When counting incrementally, the output will be set ON when the value in register **CV** reaches that held in register **PV**. When counting decrementally, the output will be set ON when the value in register **CV** reaches 0. The contents of register **PV** are unchanged after the operation.

Register PV:		*Register CV:*
Y001, 009, 017...113	C0001, 0009, 0017...1009	V0001...V0064
X001, 009, 017...113	WC001...512	
WY01...16	V0001...1024	
WX01...16	Constants 0...3999	

All the variables contained in the registers **PV** and **CV** are in the range 0...65535. The hand programming device PRG-20 can display the contents of registers up to a value of 9999.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

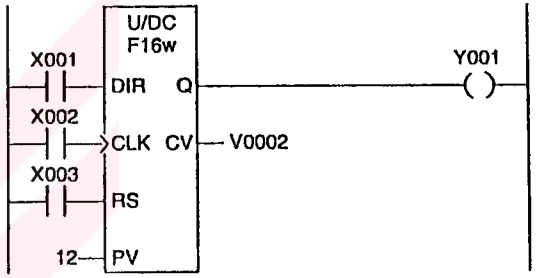
Count direction: The count direction is set by the value at the input **DIR**.
ON = up, OFF = down

Count input: Every positive edge at the input **CLK** triggers an increment/decrement of 1.

Reset input: When the input **RS** has the value logical 1, the register **CV** will be set to a value 0 if the count direction is upwards. If the count direction is downwards, the logical 1 at the input **RS** will cause the value from **PV** to be transferred into **CV**.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR      X001
STR      X002
STR      X003
F16_CNT  V0002  0012
OUT      Y001
```

The switch X001 is ON, which selects incremental counting. X003 is used to set register V0002 to a value of 0. The output Y001 starts OFF. Impulses are input by X002. As soon as V0002 reaches the value 0012, the output Y001 will switch on.

If X001 is switched off, decremental counting is selected. By switching on X003, the value 0012 is written into register V0002. The output Y001 starts OFF. Impulses are input by X002. As soon as V0002 reaches the value 0, the output Y001 will switch on.

Notes

Each of the registers V0001...V0064 can be used exactly once as an accumulator in a timer, counter or up/down counter. The content of each register may be used for other purposes.
In order to utilise the comparison function CV = PV or CV = 0, the counter output must be linked to an internal or external output.
If the special internal register C0238 is set to logical 1, the contents of the registers CV for all up/down counters will be saved if there is a power failure.

End of program		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-00_END	END F00 / EN	EN 1	1	active max. 6 inactive max. 6	FUN 0 → ENTER

Function
The F-00 instruction labels the end of the program. It effects a jump to address 0. If no F-00 instruction is written into the program, it will automatically be inserted at address 3000 (address 2000 in the PCU-20 of the SESTEP 290).
Writing the F-00 instruction at the actual end of the program reduces the execution time.

Programming example

0000	STR	X010
0001	OR	C0011
0002	AND	Y012
0003	OUT	C0020
0004	STR	X013
⋮	⋮	
0980	AND	C0017
0981	OUT	Y027
0982	NOP	
0983	NOP	
0984	NOP	
⋮	⋮	
2999	NOP	
3000	F-00	END

The F-00 instruction has been inserted at address 3000. The area from 982...2999 is automatically filled with NOP (no operation). A NOP instruction takes 1,09 µs to execute.

0000	STR	X010
0001	OR	C0011
0002	AND	Y021
0003	OUT	C0022
0004	STR	X013
⋮	⋮	
0980	AND	C0017
0981	OUT	Y027
0982	F-00	END
0983	NOP	
0984	NOP	
⋮	⋮	
2999	NOP	
3000	F-00	END

The F-00 instruction has been written into the program at address 982. This reduces the execution time.

Notes
If there is more than one F-00 instruction in a program, only the first one will be recognised.
An F-00 instruction may not be subject to any control condition.

Main circuit start (Master Control Set)		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-01_MCS	MCS F01 / EN	EN 1	1	active max. 12 inactive max. 10	FUN 1 → ENTER

Function
The F-01 instruction labels the start of the main functional circuit. If the control condition EN is ON, the instructions between the F-01 (MCS) and the F-02 (MCR) will be executed. If the control condition **EN** is OFF, the outputs between the F-01 (MCS) and the F-02 (MCR) will be set OFF.

Notes
It is not permissible to link counters, timers, outputs or functions directly to the F-01 (MCS) instruction.
If there are a number of F-01 (MCS) instructions before an F-02 (MCR) instruction, the latter will reset them all.

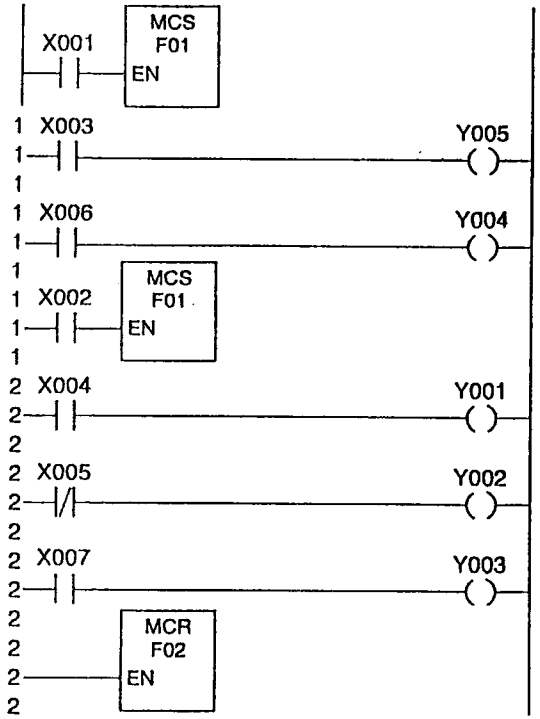
Main circuit return (Master Control Reset)		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-02_MCR	MCR F02 / EN	EN 1	1	active max. 9 inactive max. 9	FUN 2 → ENTER

Function
The F-02 instruction labels the end of the main functional circuit. This instruction is used in combination with the F-01 (MCS) instruction.

Notes
An F-02 (MCR) instruction may not be subject to any control condition.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR        X001
F-01_MCS
STR        X003
OUT        Y005
STR        X006
OUT        Y004
STR        X002
F-01_MCS
STR        X004
OUT        Y001
STR NOT    X005
OUT        Y002
STR        X007
OUT        Y003
F-02_MCR
```

If the control condition X001 is OFF, the instructions down to F-02 will have no effect which means that all outputs are switched off. If the control condition is ON, the branches down to the second main functional circuit will be activated. If the control condition for the second main circuit is ON, then all the branches will be active.

Jump circuit start (Jump Control Set)		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-03_JCS	JCS F03 EN	EN 1	1	active max. 12 inactive max. 10	FUN 3 → ENTER

EN = Control condition

Function
The F-03 instruction labels the start of a jump. If the control condition EN is ON, the instructions between the F-03 (JCS) and the F-04 (JCR) will be regarded as NOP. The contents of all registers and the status of the outputs which are skipped will remain unaltered.

Notes
It is not permissible to link counters, timers, outputs or functions directly to the F-03 (JCS) instruction. If there are a number of F-03 (JCS) instructions before an F-04 (JCR) instruction, the latter will reset them all. The special internal registers C0241...C0244 will be set OFF during the jump.

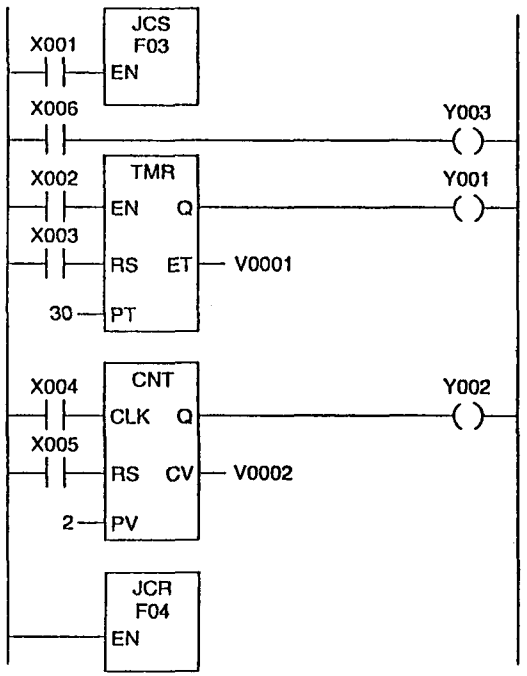
Jump circuit return (Jump Control Reset)		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-04_JCR	JCR F04 EN		1	active max. 9 inactive max. 9	FUN 4 → ENTER

Function
The F-04 instruction labels the end of a jump.This instruction is used in combination with the F-03 (JCS) instruction.

Notes
An F-00 (END) instruction between the F-03 (JCS) and the F-04 (JCR) will be recognised, irrespective of the jump status.
An F-04 instruction may not be subject to any control condition.

Programming example 1

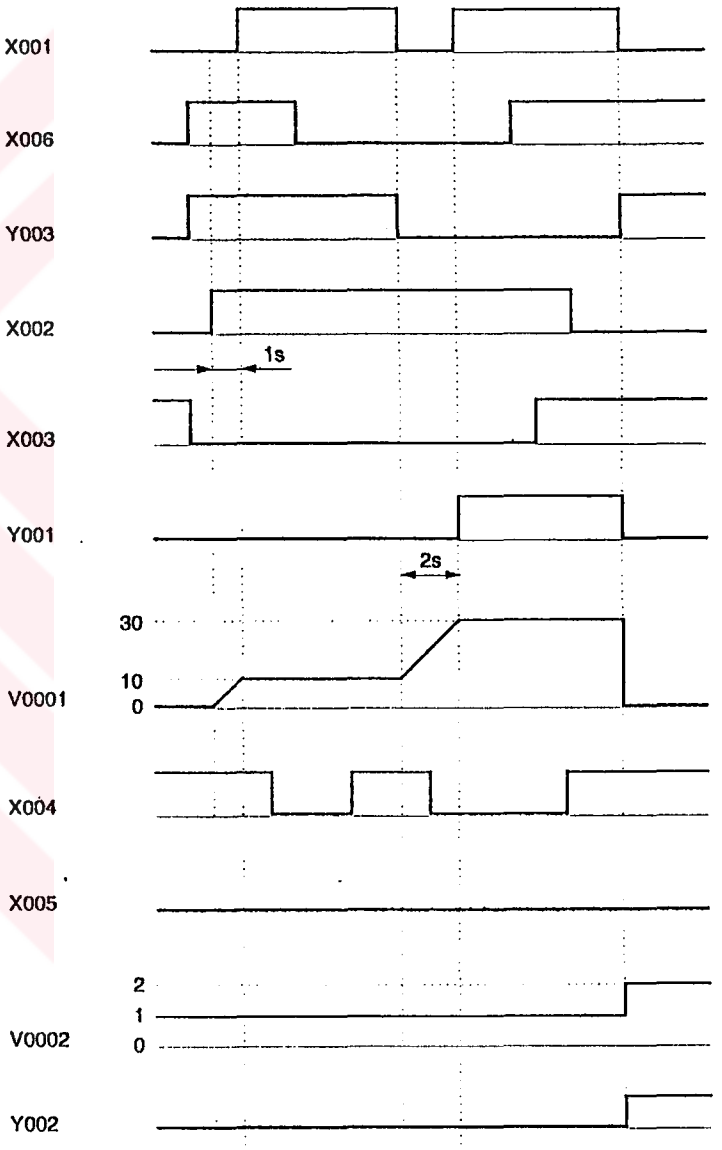
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

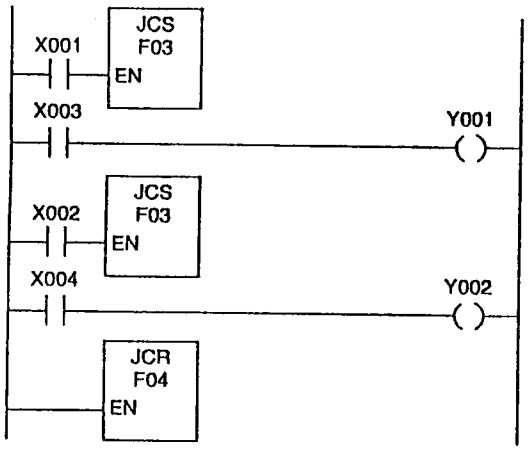
STR	X001	
F-03_JCS		
STR	X006	
OUT	Y003	
STR	X002	
STR	X003	
TMR	V0001	0030
OUT	Y001	
STR	X004	
STR	X005	
CNT	V0002	0002
OUT	Y002	
F-04_JCR		

Timing diagram for programming example 1



Programming example 2

Ladder Diagram
Programming software PRS-21:



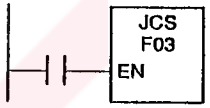
Instruction List
Programming device PRG-20/21:

```
STR         X001
F-03_JCS
STR         X003
OUT         Y001
STR         X002
F-03_JCS
STR         X004
OUT         Y002
F-04_JCR
```

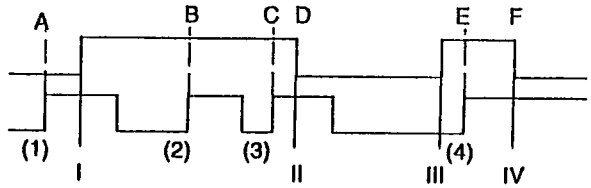
If the control condition X001 is ON, the instructions up to the F-04 (JCR) instruction are regarded as NOP and skipped. If the control condition X001 is OFF, the circuits up to the second F-03 (JCS) instruction are executed. If the control condition X002 of the second jump control is ON, the instructions up to the F-04 (JCR) instruction are skipped.
Both F-03 (JCS) instructions are reset by the same F-04 (JCR) instruction.
The special internal registers C0241...C0244 are set OFF during the jump.

Notes
For instructions which are initiated by an edge, the following must be taken into account:

Control condition 1



Control condition 2



A. The instruction will be executed when control condition 2 changes from OFF to ON (1).

B, C. The instruction will not be executed when control condition 2 changes from OFF to ON (2) or (3), because F-03 (JCS) is active.

D. The control condition 1 for the F-03 (JCS) changes from ON to OFF. However, as the signal for control condition 2 is the same at points I and II, the instruction will not be executed.

E. The instruction will not be executed, as F-03 (JCS) is active.

F. The control condition 1 for the F-03 (JCS) changes from ON to OFF. The instruction will now be executed, because the control condition 2 has changed between points III and IV from OFF to ON, which is regarded as an edge.

The special internal registers C0241...C0244 are reset when the F-03 (JCS) instruction is active.

Start of SKIP		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-07_SKIP	SKIP F07 EN	EN 1	1	active max. 21 inactive max. 11	FUN 7 → ENTER

EN = Control condition

Function

If the control condition **EN** is ON, the instructions between the F-07 (SKIP) and the F-08 (ENDS) are skipped. In contrast to the use of the F-03 (JCS) and the F-04 (JCR), this instruction does not cause the instructions between the F-07 (SKIP) and the F-08 (ENDS) to be regarded as NOP instructions, but they are genuinely skipped. The F-07 (SKIP) instruction reduces the execution time.

End of SKIP		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-08_ENDS	ENDS F08 EN		1	active max. 107 inactive max. 10	FUN 8 → ENTER

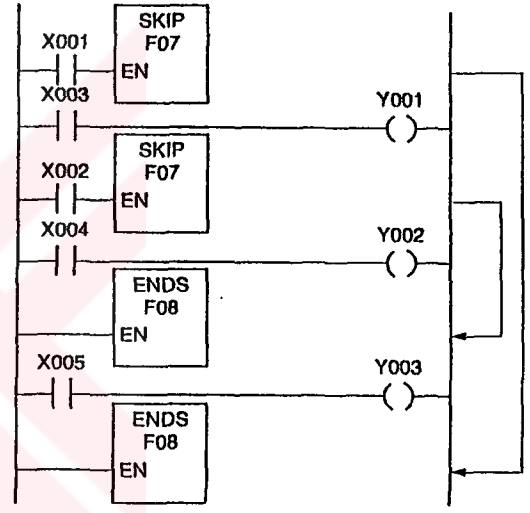
Function

The F-08 instruction labels the end of a skip. This instruction is used in combination with the F-07 (SKIP). There has to be an F-08 (ENDS) instruction programmed for each F-07 (SKIP) instruction.

An F-08 instruction may not be subject to any control condition.

Programming example 1

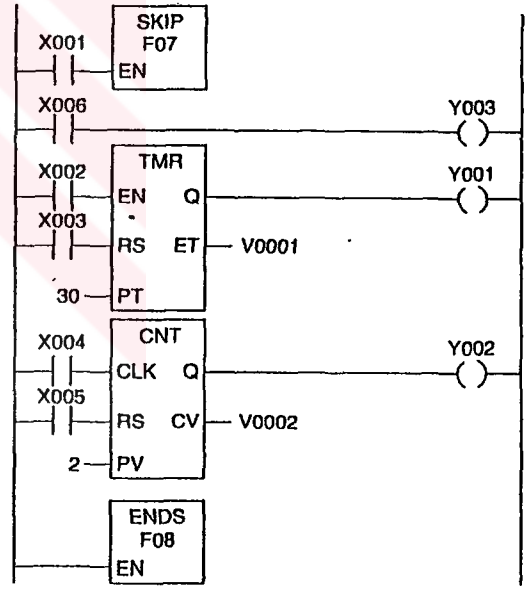
Ladder Diagram PRS-21:



Instruction List PRG-20/21:

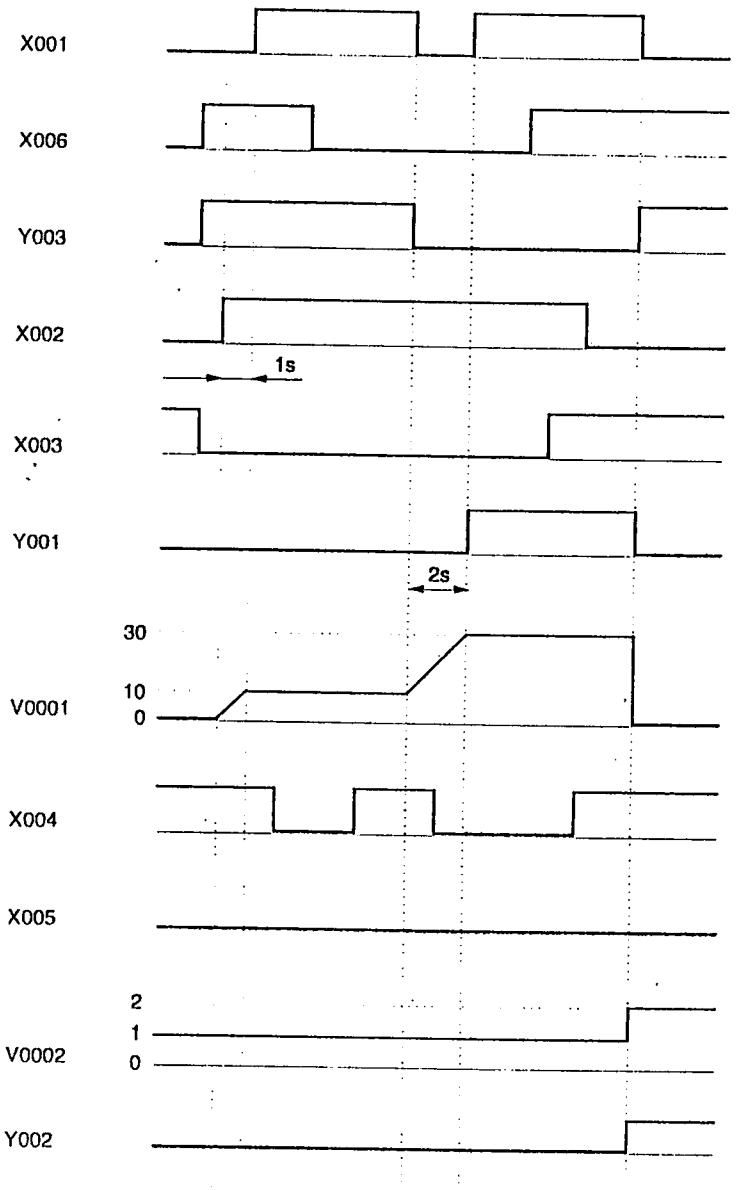
```
STR         X001
F-07_SKIP
STR         X003
OUT         Y001
STR         X002
F-07_SKIP
STR         X004
OUT         Y002
F-08_ENDS
STR         X005
OUT         Y003
F-08_ENDS
```

Programming example 2




```
STR         X001
F-07_SKIP
STR         X006
OUT         Y003
STR         X002
STR         X003
TMR         V0001   0030
OUT         Y001
STR         X004
STR         X005
CNT         V0002   0002
OUT         Y002
F-08_ENDS
```

Timing diagram for programming example 2



16 bit swap		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-09wSWAP	SWAP F09w TR REG	TR ↑	**2**	active min. **62** max. **99** inactive min. **28** max. **28**	FUN 9 w → Operand REG ENTER

TR = Control condition
REG = Swap register

Function
In register **REG** the L byte and the H byte are swapped when the signal **TR** changes from OFF to ON.

Register REG:

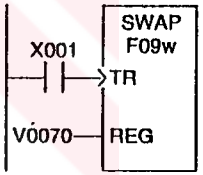
Y001, 009, 017...113 C0001, 0009, 0017...1009
WY01...16 V0001...1024
WX01...16

All variables contained in the register REG are in the range 0...65535. The hand programming device PRG-20 can display the content of register REG up to a value of 9999.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR X001
F-09wSWAP V0070

V0070 before the operation:

00001010	10011111

F-09w
SWAP

V0070 after the operation:

10011111	00001010

16 bit register shift, bi-directional		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-10wSFR	SHFR F10w DIR IN CLK RST REG	CLK ↑	**2**	active min. **103** max. **143** inactive min. **32** max. **32**	FUN 1 0 W → Operand REG ENTER

DIR = Shift direction: OFF = MSB --> LSB, ON = LSB --> MSB
IN = Data input
CLK = Control condition
RST = Reset input
REG = Working register
LSB = Least significant bit in the data word, 1st bit.
MSB = Most significant bit in the data word, 16th bit.

Function

Whilst the reset register **RST** is set OFF, a positive edge at the input **CLK** will cause the contents of register **REG** to be shifted one place towards the **LSB** or the **MSB**. The direction of shift is determined by the signal at the input **DIR**. If the reset input **RST** is set ON, all the bits of register **REG** will be set to logical 0.

*Register **REG**:*

Y001, 009, 017...113	C0001, 0009, 0017...1009
X001, 009, 017...113	V0001...1024
WY01...16	
WX01...16	

All the variables contained in register REG are in the range 0...65535.
The hand programming device PRG-20 can display the content of register REG up to a value of 9999.

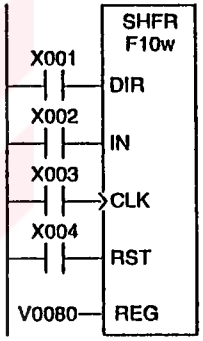
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
RST = OFF	1 or 0	1 or 0	1 or 0	0
RST = ON	0	0	0	0
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR       X001
STR       X002
STR       X003
STR       X004
F-10wSFR  V0080
```

As soon as the input X003 changes from OFF to ON, the contents of register V0080 will be shifted one place towards the LSB or the MSB. The direction of shift will be determined by the status of X001.

Register V0080 before the operation	Register V0080 after the operation	NC C0241	C C0242	Z C0243		Input condition
0000000000000000	0000000000000000	1	0	1	}	X001 = 0
0100000001000100	0010000000100010	1	0	0	}	X002 = 0
0001000001000001	0000100000100000	0	1	0	}	X003 = ↑
0000000000000001	0000000000000000	0	1	1	}	X004 = 0
0000000000000000	0000000000000000	1	0	1	}	X001 = 1
0001000001000000	0010000010000000	1	0	0	}	X002 = 0
1000000000010000	0000000000100000	0	1	0	}	X003 = ↑
1000000000000000	0000000000000000	0	1	1	}	X004 = 0
1000000000010000	1100000000001000	1	0	0	}	X001 = 0
0000000001000001	1000000000100000	0	1	0	}	X002 = 1 X003 = ↑ X004 = 0
0001000000000000	0010000000000001	1	0	0	}	X001 = 1
1000000000010000	0000000000100001	0	1	0	}	X002 = 1 X003 = ↑ X004 = 0
0000010001000000	0000000000000000	0	0	0	>	X004 = 1

8 bit transfer		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-11_XFER	XFER F11 >EN FRM TO	EN ↑	3	active min. 63 max. 92 inactive min. 41 max. 41	FUN 1 1 → Operand TO → Operand FRM ENTER

EN = Control condition **TO** = Transfer to
FRM = Transfer from

Function
The content of register **FRM** (L byte) will be copied into register **TO** (L byte) as soon as the signal **EN** changes from OFF to ON. After the operation, the contents of the register **FRM** and the H byte of the register **TO** are unaltered.

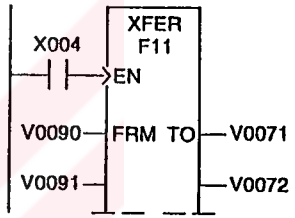
Register FRM:	*Register TO:*
Y001, 009, 017...121	Y001, 009, 017...121
X001, 009, 017...121	
WY01...16	WY01...16
WX01...16	WX01...16
C0001, 0009, 0017...1017	C0001, 0009, 0017...1017
WC001...WC512	
V0001...1024	V0001...1024
Constants 0...255	

All the variables contained in the registers TO and FRM are in the range 0...255.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Programming example

Ladder Diagram
Programming software PRS-21:



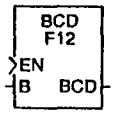
Instruction List
Programming device PRG-20/21:

```
STR          X004
F-11_XFER    V0071  V0090
F-11_XFER    V0072  V0091
```

When a positive edge is received from input X004, register V0090 (L byte) will be copied into register V0071, and register V0091 (L byte) into register V0072.

Register	*Content*	*Value*	*Register*	*Content*	*Value*
V0090	0001011101110101	6005	V0091	1000110100111010	36154
↓	↓		↓	↓	
V0071	1111000101110101	61813	V0072	0011101000111010	14906
	unchanged copied			unchanged copied	

Notes
It is possible to link up to 7 F-11 instructions to the same control condition.

8 bit binary to BCD		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-12_BCD		EN ↑	**3**	active min. **77** max.**108** inactive min. **41** max. **41**	FUN 1 2 → Operand BCD → Operand B ENTER

EN = Control condition **BCD** = Output register
B = Binary value

Function
The content of register **B** (L byte) will be converted to BCD code and saved in the register **BCD** (L byte) as soon as the signal **EN** changes from OFF to ON. After the operation, the content of the register **B** and the H byte of the register **BCD** are unaltered.

Register B:	*Register BCD:*
Y001, 009, 017...121	Y001, 009, 017...121
X001, 009, 017...121	
WY01...16	WY01...16
WX01...16	WX01...16
C0001...1017	C0001...1017
WC001...512	
V0001...1024	V0001...1024
Constants 0...99	

All the variables contained in register BCD are in the range 0...99H.
All the variables contained in register B are in the range 0...99.

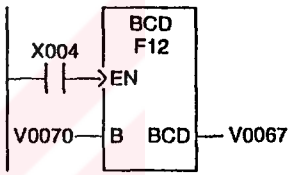
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
B < 100	x	x	x	0
B > 99	x	x	x	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



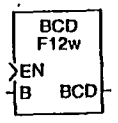
Instruction List
Programming device PRG-20/21:

```
STR        X004
F-12_BCD   V0067   V0070
```

When a positive edge is received from input X004, the content of register V0070 (L byte) will be converted to a BCD value and saved in register V0067 (L byte).

Register	*Content*	*Value*
V0070 L byte	00101011	43 decimal
↓	↓	
V0067 L byte	01000011	43 BCD
	1 digit 1 digit	

Notes
If the content of register B (L byte) exceeds 99, the operation will not be executed.

16 bit binary to BCD		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-12wBCD		EN ↑	**3**	active min. **118** max. **179** inactive min. **41** max. **41**	FUN 1 2 w → Operand BCD → Operand B ENTER

EN = Control condition **BCD** = Output register
B = Binary value

Function
The content of register **B** will be converted to BCD code and saved in register **BCD** as soon as the signal **EN** changes from OFF to ON. After the operation, the register **B** is unaltered.

Register B:	*Register BCD:*
Y001, 009, 017...113	Y001, 009, 017...113
X001, 009, 017...113	
WY01...16	WY01...16
WX01...16	WX01...16
C0001, 0009, 0017...1009	C0001, 0009, 0017...1009
WC001...512	
V0001...1024	V0001...1024
Constants 0...3999	

All the variables contained in register BCD are in the range 0...9999H.
All the variables contained in register B are in the range 0...9999.

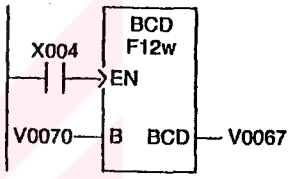
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
B < 10000	x	x	x	0
B > 9999	x	x	x	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



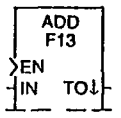
Instruction List
Programming device PRG-20/21:

```
STR      X004
F-12wBCD V0067 V0070
```

When a positive edge is received from input X004, the contents of register V0070 will be converted to a BCD value and saved in register V0067.

Register	*Content*	*Value*
V0070	0010011010110001	9905 decimal
↓	↓	
V0067	1001100100000101	9905 BCD
	1 digit .... 1 digit	

Notes
If the content of register B exceeds 9999, the operation will not be executed.

8 bit addition		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-13_ADD		EN	**3**	active min. **115** max. **148** inactive min. **51** max. **56**	FUN 1 3 → Operand TO → Operand IN ENTER

EN = Control condition **TO** = Addend 2
IN = Addend 1

Function
The content of register **TO** (L byte) will be added to the content of register **IN** (L byte) as soon as the signal **EN** changes from OFF to ON. The result is stored in register **TO+1** (L byte). After the operation, the contents of the registers **IN, TO** and **TO+1** (H byte) will be unaltered.

Register IN:	*Register TO:*
Y001, 009, 017...121	Y001, 009, 017...113
X001, 009, 017...121	
WY01...16	WY01...15
WX01...16	WX01...15
C0001, 0009, 0017...1017	C0001, 0009, 0017...1009
WC001...512	
V0001...1024	V0001...1023
Constants 0...99	

All the variables contained in the registers **IN** and **TO** are in the range 0...99.

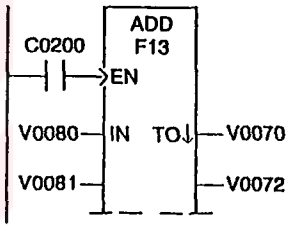
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
0	1	0	1	0
1...99	1	0	0	0
100	0	1	1	0
> 100	0	1	0	0
IN or TO > 99	0	0	0	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	C0200	
F-13_ADD	**V0070**	**V0080**
F-13_ADD	**V0072**	**V0081**

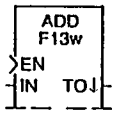
On detecting the positive edge from the internal register C0200, the L byte of the register V0070 will be added to the L byte of the register V0080, and the result will be stored in the L byte of the register V0071. Afterwards the L byte of the register V0072 will be added to the content of register V0081, and the result stored in the L byte of the register V0073.

Register	*Content*	*Value*	*Register*	*Content*	*Value*
C0242	0	0	C0242	0	0
+ V0080 L byte	0 0 0 1 1 1 1 0	30	+ V0081 L byte	0 0 1 0 0 0 1 0	34
+ V0070 L byte	0 0 1 1 0 0 1 0	50	+ V0072 L byte	0 1 0 1 1 1 1 1	95
= V0071 L byte	0 1 0 1 0 0 0 0	80	= V0073 L byte	0 0 0 1 1 1 0 1	29
C0242	0	0	C0242	1	1

The result is less than 100, and is contained completely in the register V0071, so that the special internal register C0242 is not set.

The result exceeds the value 100, and hence the register V0073 will contain only the amount by which it exceeds 100. The special internal register C0242 is set.

Notes
If the content of register TO or IN exceeds 99, the operation will not be executed.
The special internal registers C0241...C0244 may be affected by other operations in the same program.
It is possible to link up to 7 F-13 instructions to the same control condition. In this case, the content of the carry internal register C0242 will also be cumulated from the second F-13 instruction on. Therefore, it is recommendable to program one operation only in each instruction.

16 bit addition		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-13wADD		EN	3	active min. 134 max. 207 inactive min. 54 max. 58	FUN 1 3 w → Operand TO → Operand IN ENTER

EN = Control condition **TO** = Addend 2
IN = Addend 1

Function

The content of register **TO** will be added to the content of register **IN** as soon as the signal **EN** changes from OFF to ON. The result will be stored in the register **TO+1**. After the operation, the content of registers **IN** and **TO** will be unaltered.

Register IN:	*Register TO:*
Y001, 009, 017...113	Y001, 009, 017...097
X001, 009, 017...113	
WY01...16	WY01...15
WX01...16	WX01...15
C0001, 0009, 0017...1009	C0001, 0009, 0017...0993
WC001...512	
V0001....1024	V0001...1023
Constants 0...3999	

All the variables contained in the registers **TO** and **IN** are in the range 0...9999.

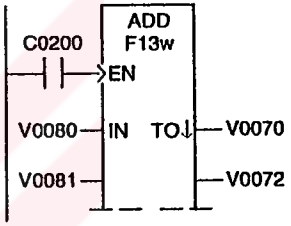
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
0	1	0	1	0
1...9999	1	0	0	0
10000	0	1	1	0
> 10000	0	1	0	0
IN or TO > 9999	0	0	0	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR          C0200
F-13w ADD    V0070   V0080
F-13w ADD    V0072   V0081
```

On detecting the positive edge of the internal register C0200, the register V0070 will be added to the content of register V0080, and the result will be stored in register V0071. Afterwards the register V0072 will be added to the content of register V0081, and the result stored in register V0073.

Register	*Content*	*Value*
C0242	0	0
+ V0080	0000000000011110	0030
+ V0070	0010011011111111	9983
= V0071	0000000000001101	0013
C0242	1	1

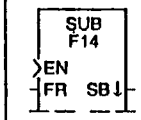
The result exceeds 10000, and hence the register V0071 will contain only the amount by which it exceeds 10000. The special internal register C0242 is set.

Register	*Content*	*Value*
C0242	1	1
+ V0081	0000000001000010	0066
+ V0072	0001000011100101	4325
= V0073	0001000100101000	4392
C0242	0	0

The resultat is less than 10000, and is contained completely in the register V0073. The carry from the preceding addition is added to the result. The special internal register C0242 is not set.

Notes

If the content of register TO or IN exceeds 9999, the operation will not be executed. The special internal registers C0241...C0244 may be affected by other operations in the same program.
It is possible to link up to 7 F-13w instructions to the same control condition. In this case, the content of the carry internal register C0242 will also be cumulated from the second F-13w instruction on. Therefore, it is recommendable to program one operation only in each instruction.

8 bit subtraction		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-14_SUB		EN ↑	**3**	active min. **120** max. **155** inactive min. **54** max. **58**	FUN 1 4 → Operand SB → Operand FR ENTER

EN = Control condition **SB** = Subtrahend
FR = Minuend

Function
The content of register **SB** (L byte) will be subtracted from the content of register **FR** (L byte) as soon as the signal **EN** changes from OFF to ON. The result is stored in register **SB+1** (L byte). After the operation, the contents of registers **FR**, **SB** and **SB+1** (H byte) will be unaltered.

Register FR:	*Register SB:*
Y001, 009, 017...121	Y001, 009, 017...113
X001, 009, 017...121	
WY01...16	WY01...15
WX01...16	WX01...15
C0001, 0009, 0017...1017	C0001, 0009, 0017...1009
WC001...512	
V0001...1024	V0001...1023
Constants 0 ...99	

All the variables contained in the registers **SB** and **FR** are in the range 0...99.

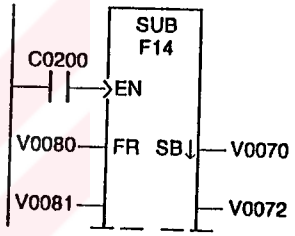
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
1...99	1	0	0	0
0	1	0	1	0
< 0	0	1	0	0
FR or SB > 99	0	0	0	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	C0200	
F-14_SUB	**V0070**	**V0080**
F-14_SUB	**V0072**	**V0081**

On detecting the positive edge from the internal register C0200, the L byte of the register V0070 will be subtracted from the L byte of the register V0080, and the result will be stored in the L byte of the register V0071. Afterwards the L byte of the register V0072 will be subtracted from the content of register V0081, and the result stored in the L byte of the register V0073.

Register		*Content*	*Value*
V0080	L byte	0 1 0 0 1 0 0 1	73
- V0070	L byte	0 0 1 0 0 0 0 1	33
- C0242		0	0
= V0071	L byte	0 0 1 0 1 0 0 0	40
C0242		0	0

The result is greater than 00 (a positive value) and is held in the register V0071. The special internal register C0242 is set OFF.

Register		*Content*	*Value*
V0081	L byte	0 0 1 1 1 0 1 1	59
- V0072	L byte	0 1 0 0 0 1 1 1	71
- C0242		0	0
= V0073	L byte	0 1 0 1 1 0 0 0	88
C0242		1	1

The result is less than 00 (a negative value). The result is stored as the complementary value to 100 in the register V0073. The special internal register C0242 is set ON.

Notes
If the content of register FR or SB exceeds 99, the operation will not be executed.
The special internal registers C0241... C0244 may be affected by other operations in the same program.
It is possible to link up to 7 F-14 instructions to the same control condition. In this case, the content of the carry internal register C0242 will also be subtracted from the second F-14 instruction on.

16 bit subtraction		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-14wSUB	SUB F14w EN FR SB	EN	3	active min. 137 max. 193 inactive min. 54 max. 58	FUN 1 4 w → Operand SB → Operand FR ENTER

EN = Control condition
FR = Minuend
SB = Subtrahend

Function

The content of register **SB** will be subtracted from the content of register **FR** as soon as the signal EN changes from OFF to ON. The result is stored in register **SB+1**. After the operation, the contents of registers **FR** and **SB** will be unaltered.

Register FR:	*Register SB:*
Y001, 009, 017...113	Y001, 009, 017...097
X001, 009, 017...113	
WY01...16	WY01...15
WX01...16	WX01...15
C0001, 0009, 0017...1009	C0001, 0009, 0017...0993
WC001...512	
V0001...1024	V0001...1023
Constants 0...3999	

All the variables contained in the registers **FR** and **SB** are in the range 0...9999.

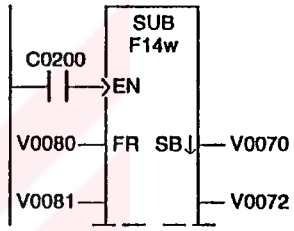
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
1...9999	1	0	0	0
0	1	0	1	0
< 0	0	1	0	0
FR or SB > 9999	0	0	0	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	C0200	
F-14wSUB	**V0070**	**V0080**
F-14wSUB	**V0072**	**V0081**

On detecting the positive edge from the internal register C0200, the register V0070 will be subtracted from the register V0080, and the result will be stored in the register V0071. Afterwards the register V0072 will be subtracted from the register V0081, and the result stored in the register V0073.

Register	*Content*	*Value*	*Register*	*Content*	*Value*
V0080	0000000101000000	0320	V0081	0000000000111110	0062
- V0070	0000000111000111	0455	- V0072	0000000000101111	0047
- C0242	0	0	- C0242	1	1
= V0071	0010011010001001	9865	= V0073	0000000000001110	0014
C0242	1	1	C0242	0	0

The result is less than 0000 (a negative value). The result is stored as the complementary value to 10000 in the register V0071. The special internal register C0242 is set ON.

The result is greater than 0000 (a positive value) and is held in the register V0073. The special internal register C0242 is set OFF.

Notes

If the content of register FR or SB exceeds 9999, the operation will not be executed.
The special internal registers C0241... C0244 may be affected by other operations in the same program.
It is possible to link up to 7 F-14 instructions to the same control condition. In this case, the content of the carry internal register C0242 will also be subtracted from the second F-14w instruction on.

8 bit comparison		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-15_CMP	CMP F15 EN IN TO	EN 1	**3**	active max. **95** inactive max. **44**	FUN 1 5 → Operand (TO) → Operand (IN) ENTER

EN = Control condition
IN = Comparison register
TO = Comparison register

Function

The content of the register IN (L byte) will be compared with the content of the register TO (L byte) to see if it is =, < or >, provided that the signal EN is ON. The result is stored in the special internal registers C0241...C0243. After the operation, the contents of the registers IN and TO will be unaltered.

Register IN:	*Register TO:*
Y001, 009, 017...121	Y001, 009, 017...121
X001, 009, 017...121	X001, 009, 017...121
WY01...16	WY01...16
WX01...16	WX01...16
C0001, 0009, 0017...1017	C0001, 0009, 0017...1017
WC001...512	
V0001...1024	V0001...1024
Constants 0...255	

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

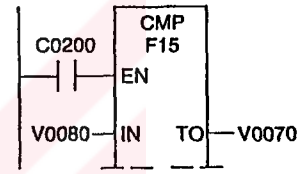
Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
IN (L byte) = TO (L byte)	1	0	1	0
IN (L byte) > TO (L byte)	1	0	0	0
IN (L byte) < TO (L byte)	0	1	0	0
Without execution of the operation	0	0	0	0

Notes

These special internal registers must be validated immediately after the operation.
It is possible to link up to 7 F-15 instructions to the same control condition.

Programming example

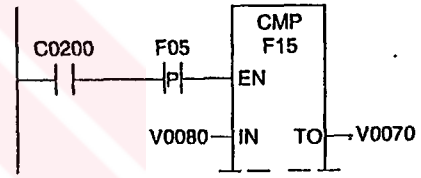
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

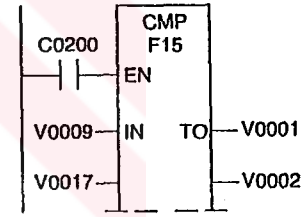
```
STR          C0200
F-15_CMP     V0070  V0080
```

As long as the internal register C0200 is set to ON, the L byte of register V0080 will be compared with the L byte of register V0070 on each cycle through the program. The result is written into the special internal registers C0241...C0243.




```
STR          C0200
F-05_DIFO
F-15_CMP     V0070  V0080
```

In order to make the comparison function dependent on an event it can, for example, be linked to an edge detection. This has the effect that the L byte of register V0080 will then only be compared with the L byte of register V0070 when the internal register C0200 changes from OFF to ON.

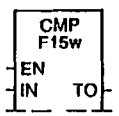



```
STR          C0200
F-15_CMP     V0001  C0009
F-15_CMP     V0002  C0017
```

In order to compare items of data which are longer than 1 byte, several F-15 instructions can be linked to the same input condition. In this case, the carry internal register C0242 will also be taken into account from the second F-15 instruction on.

Notes

The special internal registers C0241...C0243 may be affected by other operations in the same program.

16 bit comparison		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-15wCMP		EN 1	**3**	active max. **95** inactive max. **44**	FUN 1 5 w → Operand (TO) → Operand (IN) ENTER

EN = Control condition **TO** = Comparison register
IN = Comparison register

Function
The content of the register **IN** will be compared with the content of the register **TO** to see if it is =, < or >, provided that the signal **EN** is ON. The result is stored in the special internal registers C0241...C0243. After the operation, the contents of the registers **IN** and **TO** will be unaltered.

*Register **IN**:*	*Register **TO**:*
Y001, 009, 017...113	Y001, 009, 017...113
X001, 009, 017...113	X001, 009, 017...113
WY01...16	WY01...16
WX01...16	WX01...16
C0001, 0009, 0017...1009	C0001, 0009, 0017...1009
WC001...512	WC001...512
V0001...1024	V0001...1024
Constants 0...3999	

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

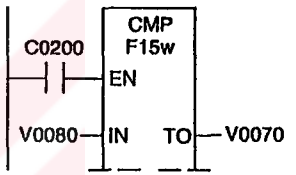
Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
IN = TO	1	0	1	0
IN > TO	1	0	0	0
IN < TO	0	1	0	0
Without execution of the operation	0	0	0	0

Notes
These special internal registers must be validated immediately after the operation.
It is possible to link up to 7 F-15w instructions to the same control condition.

Programming example

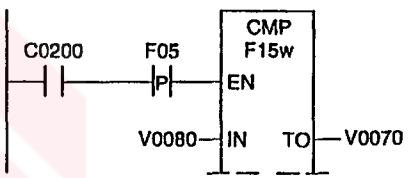
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

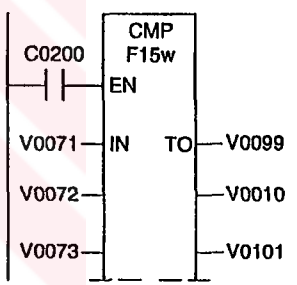
STR	C0200	
F-15w_CMP	**V0070**	**V0080**

As long as the internal register C0200 is set to ON, the register V0080 will be compared with the register V0070 on each cycle through the program. The result is written into the special internal registers C0241...C0243.



STR	C0200	
F-05_DIFO		
F-15w_CMP	**V0070**	**V0080**

In order to make the comparison function dependent on an event it can, for example, be linked to an edge detection. This has the effect that the register V0080 will then only be compared with the register V0070 when the internal register C0200 changes from OFF to ON.



STR	C0200	
F-15w_CMP	**V0099**	**V0071**
F-15w_CMP	**V0100**	**V0072**
F-15w_CMP	**V0101**	**V0073**

In order to compare items of data which are longer than 1 word, several F-15w instructions can be linked to the same input condition. In this case, the carry internal register C0242 will also be taken into account from the second F-15w instruction on.

Notes
The special internal registers C0241...C0243 may be affected by other operations in the same program.

8 bit BCD to binary		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-17_BIN	BIN F17 >EN BCD B	EN	3	active min. 84 max. 117 inactive min. 45 max. 45	FUN 1 7 → Operand B → Operand BCD ENTER

EN = Control condition **B** = Output register
BCD = BCD value

Function
The BCD number in the register **BCD** (L byte) will be converted to a binary number and saved in the register **B** (L byte) when the signal **EN** changes from OFF to ON. After the operation, the content of the register **BCD** and the H byte of register **B** will be unaltered.

*Register **BCD**:*	*Register **B**:*
Y001, 009, 017...121	Y001, 009, 017...121
X001, 009, 017...121	
WY01...16	WY01...16
WX01...16	WX01...16
C001, 009, 017...1017	C001, 009, 017...1017
WC001...512	
V001...1024	V001...1024
Constants 0...99	

All the variables contained in the register BCD are in the range 0...99H.
All the variables contained in the register B are in the range 0...99.

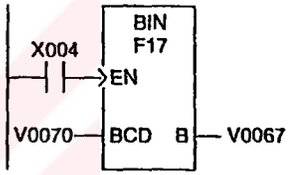
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
BCD < 100H	x	x	x	0
BCD > 99H	x	x	x	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X004	
F-17_BIN	**V0067**	**V0070**

When a positive edge is received from the input X004, the BCD number in the L byte of register V0070 will be converted to a binary number and saved in the register V0067 (L byte).

Register	*Content*	*Value*
V0070 L byte	01000011	43 BCD
	1 digit 1 digit	
V0067 L byte	00101011	43 decimal

Notes
If the content of the register BCD (L byte) exceeds 99H, the operation will not be executed.

16 bit BCD to binary		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-17wBIN	BIN F17w EN BCD B	EN	**3**	active min. **118** max. **179** inactive min. **41** max. **41**	FUN 1 7 w → Operand B → Operand BCD ENTER

EN = Control condition **B** = Output register
BCD = BCD value

Function
The BCD number in the register **BCD** will be converted to a binary number and saved in the register **B** when the signal **EN** changes from OFF to ON. After the operation, the content of the register **BCD** will be unaltered.

Register BCD:	*Register B:*
Y001, 009, 017...113	Y001, 009, 017...113
X001, 009, 017...113	
WY01...16	WY01...16
WX01...16	WX01...16
C0001, 0009, 0017...1009	C0001, 0009, 0017...1009
WC001...512	
V0001...1024	V0001...1024
Constants 0...3999	

All the variables contained in the register BCD are in the range 0...9999H.
All the variables contained in the register B are in the range 0...9999.

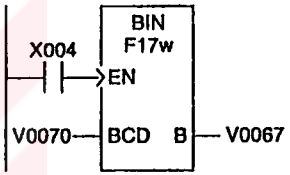
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
BCD < 10000H	x	x	x	0
BCD > 9999H	x	x	x	1
Without execution of the operation	0	0	0	0

Programming example

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR      X004
F-17wBIN V0067 V0070
```

When a positive edge is received from the input X004, the BCD number in the register V0070 will be converted to a binary number and saved in the register V0067.

Register	*Content*	*Value*
V0070	1001100100000101	9905 BCD
	1 digit .... 1 digit	
V0067	0010011010110001	9905 decimal

Notes
If the content of the register BCD exceeds 9999H, the operation will not be executed.

16 bit multiplication		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-18wMUL	MUL F18w EN MR MN↓	EN ↑	**3**	active max. **200** inactive max. **45**	FUN 1 8 w → Operand MN → Operand MR ENTER

EN = Control condition
MR = Multiplier
MN = Multiplicand

Function
When the signal **EN** changes from OFF to ON, the content of the register **MR** will be multiplied by the content of the register **MN** and the result stored in the registers **MN+2** and **MN+1**. After the operation, the contents of the registers **MR** and **MN** will be unaltered.

Register MR:
WY01...16
WX01...16
V0001...1024
WC001...512
Constants 0...3999

Register MN:
WY01...14
WX01...14
V001...1022

All the variables contained in the registers MN and MR are in the range 0...9999.

Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

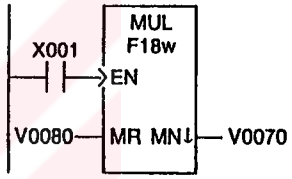
Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
MR, MN, MN+2, MN+1 < 10000	x	x	x	0
MR, MN, MN+2, MN+1 > 9999	x	x	x	1
Without execution of the operation	x	x	x	0

If MR or MN > 9999, then the error flag C0244 will be set to ON.

Programming example
Multiplication 900 x 325 = 292500

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR       X001
F-18wMUL  V0070  V0080
```

When the signal from the input X001changes from OFF to ON, the content of the register V0080 will be multiplied by the content of the register V0070. The result is stored in the registers V0072 and V0071.

Register	*Content*	*Value*		*Register*	*Content*	*Value*	
V0080	0000000101000101	325	x	V0070	0000001110000100	900	=
V0072	0000000000011101	29		V0071	0000100111000100	2500	

Notes
If the content of the register MR or MN exceeds 9999, the operation will not be executed and the error flag C0244 will be set to ON.

16 bit division		Trigg. cond.	No. of steps	Execution time µs	Input programming device
F-19wDIV	DIV F19w EN DR DN	EN ↑	3	active max. 3000 inactive max. 45	FUN 1 9 w → Operand DN → Operand DR ENTER

EN = Control condition **DN** = Dividend
DR = Divisor

Function
When the signal **EN** changes from OFF to ON, the contents of the registers **DN+1** and **DN** will be divided by the content of the register **DR** and the result stored in the registers **DN+3** and DN+2. The rest of the division will be stored in the register V0156. After the operation, the contents of the registers **DR**, **DN+1** and **DN** will be unaltered.

Register DR:	*Register DN:*
WY01...16	WY01...13
WX01...16	WX01...13
V0001...1024	V0001...1021
WC001...512	
Constants 0...3999	

All the variables contained in the registers DN, DN+1 and DR are in the range 0...9999.

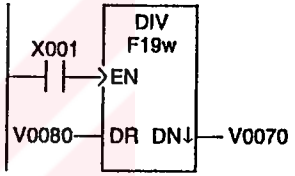
Note: The CPU module PCU-20 of the SESTEP 290 has smaller register ranges.

Table of the special internal register status:

Result after the operation:	NC C0241	C C0242	Z C0243	ERR C0244
DR, DN+1, DN < 10000 DR ≠ 0	x	x	x	0
DR, DN+1, DN > 9999 DR = 0	x	x	x	1
Without execution of the operation	0	0	0	0

Programming example
Division 292500 / 3 = 97500

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR      X001
F-19wDIV V0070 V0080
```

When the signal from the input X001 changes from OFF to ON, the contents of the registers V0071 and V0070 will be divided by the content of the register V0080. The quotient will be stored in the registers V0073 and V0072.

Register	*Content*	*Value*	*Register*	*Content*	*Value*	
V0071	0000000000011101	29	V0070	0000100111000100	2500	/
V0080	0000000000000011	3				=
V0073	0000000000001001	9	V0072	0001110101001100	7500	

Notes
If the content of the register DN or DR exceeds 9999, the operation will not be executed and the error flag C0244 will be set to ON.

Programming examples

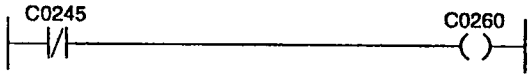
1. Analogue extension unit IOI-11 of the SESTEP 190

The analogue extension unit handles signals of 0...20 mA. If an encoder is connected which has signals of 4...20 mA, the values must be adapted. At 4 mA the content of the register WX01 must contain the value 819. This corresponds to the value 0 on the encoder. If the value is less than 819, this means a breakage in the wiring or a bad contact.

Ladder Diagram
Programming software PRS-21:

Instruction List
Programming device PRG-20/21:

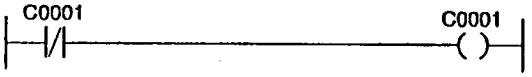
Path 1:




```
STR NOT   C0245
OUT       C0260
```

The internal register C0260 must always be switched on to have the analogue extension unit working.

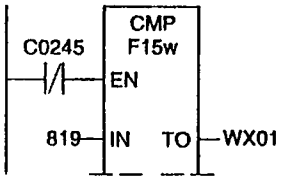
Path 2:




```
STR NOT   C0001
OUT       C0001
```

At each second program scan, the internal register C0001 produces a positive edge.

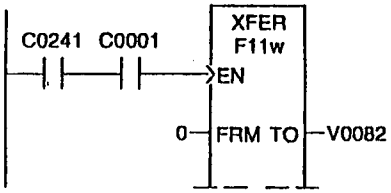
Path 3:




```
STR NOT   C0245
F-15w_CMP WX01 0819
```

The signal at the first analogue input is checked if it is greater or less than 4 mA.

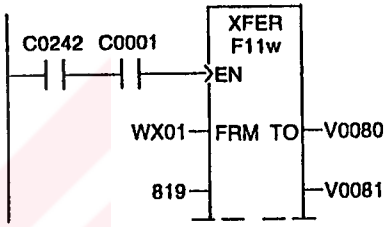
Path 4:




```
STR       C0241
AND       C0001
F-11w_XFER V0082 0000
```

If the signal is less than or equal to 4 mA, the register V0082 receives the value 0.

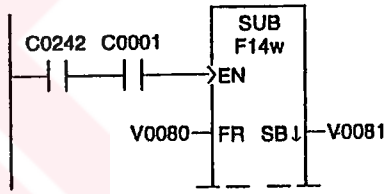
Path 5:




```
STR       C0242
AND       C0001
F-11w_XFER V0080 WX01
F-11w_XFER V0081 0819
```

If the signal is greater than 4 mA, the corresponding digital value of the signal will be transferred into the register V0080 and the digital value of 4 mA (819) into the register V0081.

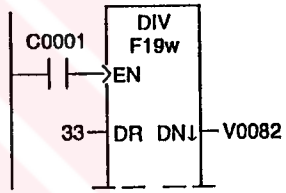
Path 6:




```
STR       C0242
AND       C0001
F-14w_SUB V0081 V0080
```

The value 819 is subtracted from the digital value of the first input. Therefore the value 0 will be present at 4 mA.

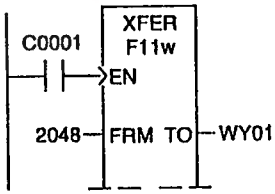
Path 7:




```
STR       C0001
F-19w_DIV Y0082 0033
```

Now, the result of the subtraction must be divided by a scaling constant to get the desired scale. For example, a scaling constant of about 33 ((4095-819)/100) is used to get a scale of 0...100 for the 4...20 mA. The result will be stored in register V0084.

Path 8:




```
STR       C0001
F-11w_XFER WY01 2048
```

If the value 2048 is transferred into the analogue output register WY01, a current of 10 mA will be flowing at the analogue output.

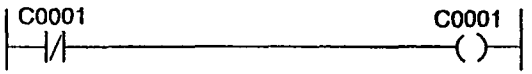
2. Analogue input modules of the SESTEP 290

The program transfers permanently the values of the input channels of an analogue module into 4 allocated registers.
The analogue input module was put into the first slot of the module housing rack.

Ladder Diagram
Programming software PRS-21:

Instruction List
Programming device PRG-20/21:

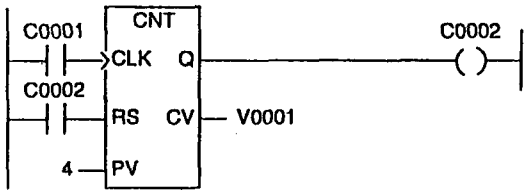
Path 1:




```
STR NOT   C0001
OUT       C0001
```

At each second program scan, the internal register C0001 produces a positive edge, which increments the register V0001 of the sequencer.

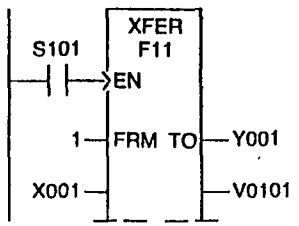
Path 2:




```
STR   C0001
STR   C0002
CNT   V0001  0002
OUT   C0002
```

At each second program scan, the register V0001 of the sequencer with the contacts S101...S116 is incremented. At reaching the value 4, the internal register C0002 resets the register in the next program scan.

Path 3:

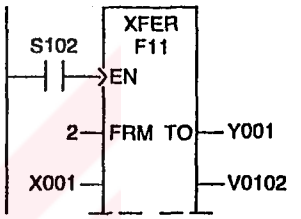


(Y1 = 1, Y2 = 0)

```
STR          S101
F-11_XFER    Y001   0001
F-11_XFER    V0101  X001
```

At the first program scan, the sequencer contact S101 will be closed. The value of the channel 1 will be transferred into the register V0101. By setting the outputs Y001 = 1, Y002 = 0, the channel 2 is selected.
The outputs are written into the I/O image memory at the end of a program scan, therefore the data of the channel 2 will be available in the second next scan only.

Path 4:

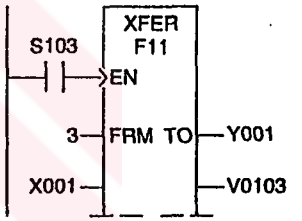


(Y1 = 0, Y2 = 1)

```
STR          S102
F-11_XFER    Y001   0002
F-11_XFER    V0102  X001
```

The value of the channel 2 is transferred into the register V0102. By setting the outputs Y001 = 0, Y002 = 1, the channel 3 is selected.

Path 5:

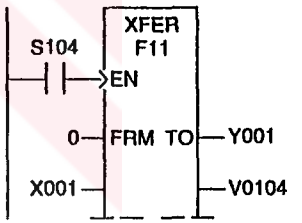


(Y1 = 1, Y2 = 1)

```
STR          S103
F-11_XFER    Y001   0003
F-11_XFER    V0103  X001
```

The value of the channel 3 is transferred into the register V0103. By setting the outputs Y001 = 1, Y002 = 1, the channel 4 is selected.

Path 6:



(Y1 = 0, Y2 = 0)

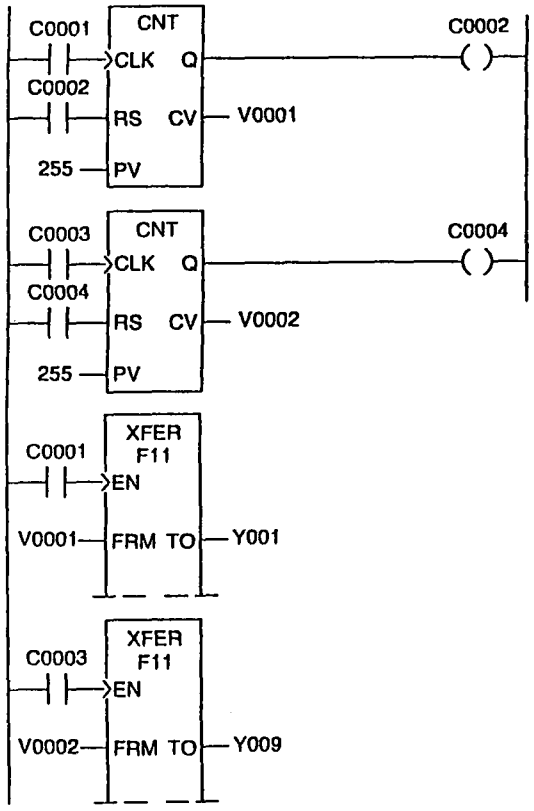
```
STR          S104
F-11_XFER    Y0001  0000
F-11_XFER    V0104  X001
```

The value of the channel 4 is transferred into the register V0104. By setting the outputs Y001 = 0, Y002 = 0, the channel 1 is selected again.

3. Analogue output modules of the SESTEP 290

Ramp generator

Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

```
STR        C0001
STR        C0002
CNT        V0001   0255
OUT        C0002

STR        C0003
STR        C0004
CNT        V0002   0255
OUT        C0004

STR        C0001
F11_XFER   Y0001   V0001

STR        C0003
F11_XFER   Y0009   V0002
```

When a positive edge of C0001 or C0003 is detected, the contents of the counters V0001 or V0002 are incremented by 1 and transferred to the analogue output channels 1 (Y001...Y008) or 2 (Y009...Y016) in the same program scan.

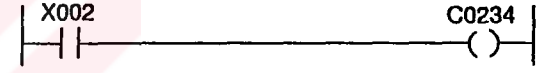
4. High-speed counter of the SESTEP 190

The program counts starting at 0 to the upper limit, which is defined by the value contained in the register WC002. There the direction of count will be changed and the program counts down to the lower limit, which is defined by the value contained in the register WC001. Afterwards the counter oscillates between the two limits until it is reset by the internal register C0235 or stopped with the internal register C0234.

Ladder Diagram
Programming software PRS-21:

Instruction List
Programming device PRG-20/21:

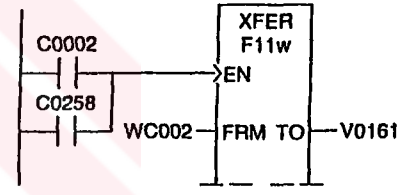
Path 1:




```
STR        X002
OUT        C0234
```

The input X002 sets the special internal register C0234 and activates the high-speed counter.

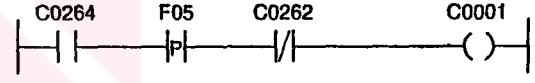
Path 2:




```
STR        C0002
OR         C0258
F-11wXFER  V0161   WC002
```

The special internal register C0258 is active during the first program scan. It is used to load the upper counter value (content of the register WC002) into the set-point register V0161. Starting with the second counting upwards, the auxiliary internal register C0002 takes this function.

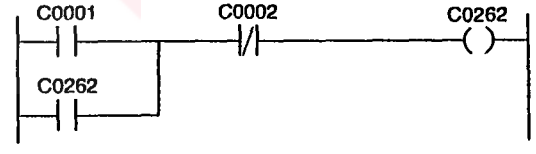
Path 3:




```
STR        C0264
F-05_DIFO
AND NOT    C0002
OUT        C0262
```

If the value of the count register V0065 reaches the upper value of the set-point register V0161, the internal register C0264 will be switched on and the auxiliary internal register C0001 will become active for one program scan.

Path 4:

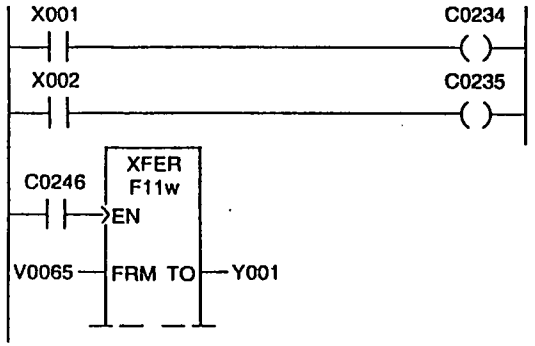



```
STR        C0001
OR         C0262
AND NOT    C0002
OUT        C0262
```

The auxiliary internal register C0001 switches the internal register C0262 to count downwards. The hold-on circuit will be reset by the auxiliary internal register C0002, after the lower limit has been reached.

5. High-speed counter of the SESTEP 290

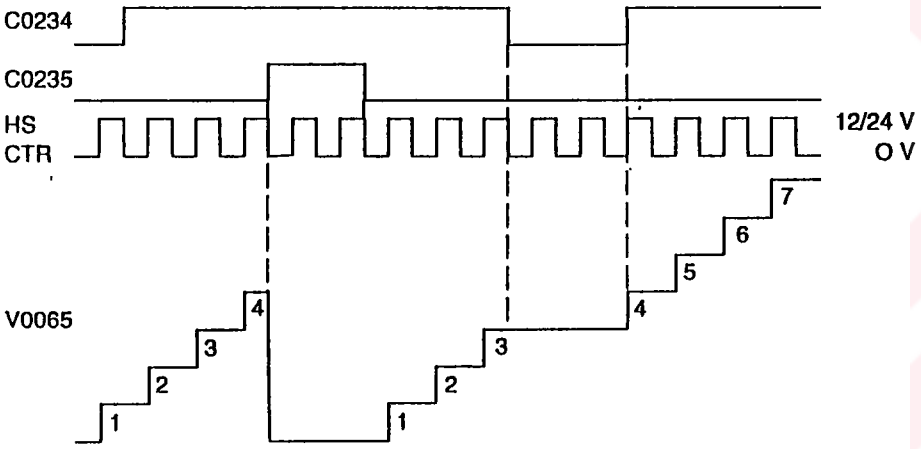
Ladder Diagram
Programming software PRS-21:



Instruction List
Programming device PRG-20/21:

STR	X001	
OUT	C0234	
STR	X002	
OUT	C0235	
STR	C0246	
F-11wXFER	Y001	V0065

X001 = ON --> counter enabled (C0234)
X002 = ON --> counter reset (C0235)
C0246 = 0,1 second scan time
Display of the HS CTR register at the outputs Y001...Y016.

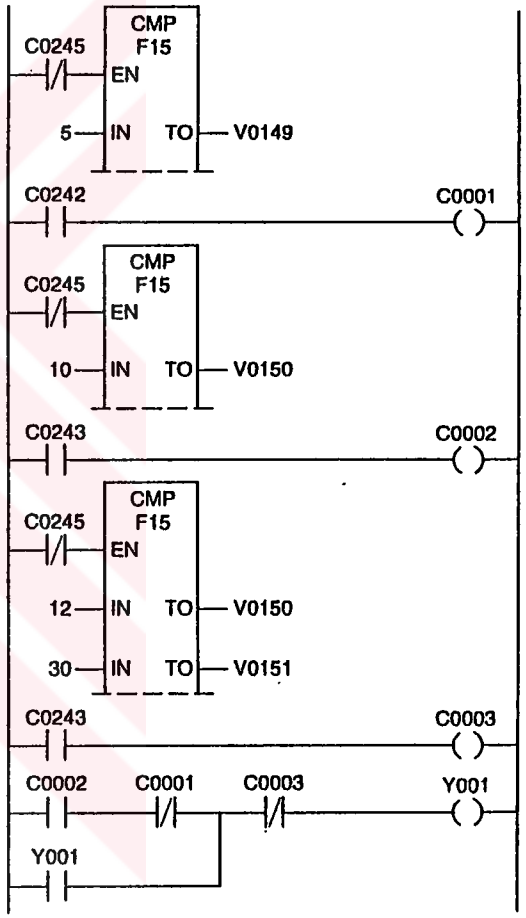


For further information about the high-speed counter of the SESTEP 290, see page 3.14

6. Real time clock

A device should be switched on every day, with the exception of Saturday and Sunday, between 10.00 and 12.30.

Ladder Diagram of the programming software PRS-21:



On Saturdays and on Sundays C0001 is switched on.
Week-day register V0149 > 5

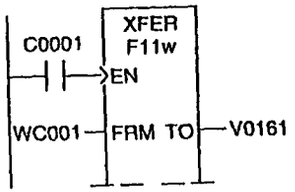
At 10.00, C0002 is switched on.
Hour register V0150 = 10

At 12.30, C0003 is switched on.
Hour register V0150 = 12
Minute register V0151 = 30

By linking the internal registers, the desired functionality is programmed.

For further information about the real time clock, see page 3.15

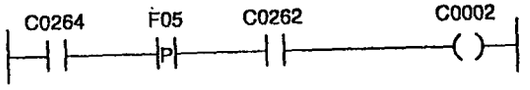
Path 5:




```
STR          C0001
F-11wXFER    V0161   WC001
```

The auxiliary internal register C0001 is used to load the lower count value (content of the register WC001) into the set-point register V0161, after the upper limit has been reached.

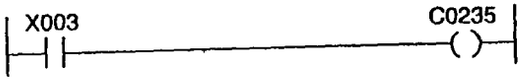
Path 6:




```
STR          C0264
F-05_DIFO
AND          C0262
OUT          C0002
```

If the value of the count register V0065 reaches the lower limit in the set-point register C0161, the internal register C0264 will be switched on and the auxiliary internal register C0002 will become active for one program scan.

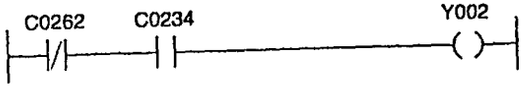
Path 7:




```
STR          X003
OUT          C0235
```

If the input X003 is switched on, the special internal register C0235 will set the high-speed counter to 0.

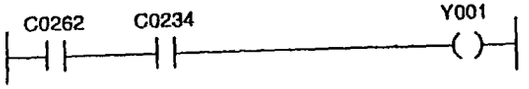
Path 8:




```
STR NOT      C0262
AND          C0234
OUT          Y002
```

The enabled counter sets the output Y002 to on, when counting upwards.

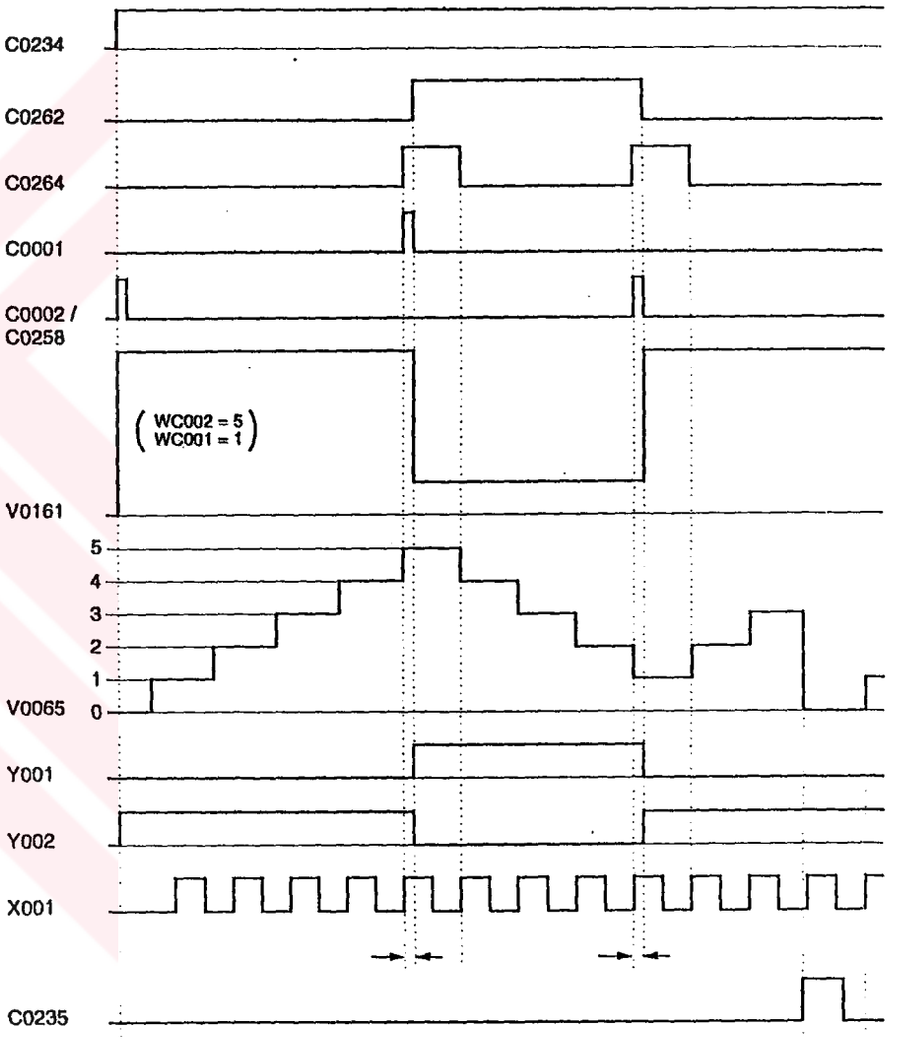
Pfad 9:




```
STR          C0262
AND          C0234
OUT          Y001
```

The enabled counter sets the output Y001 to on, when counting downwards.

Timing diagram



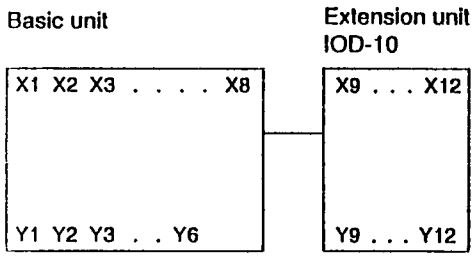
For further information about the high-speed counter of the SESTEP 190, see page 3.12

Addressing

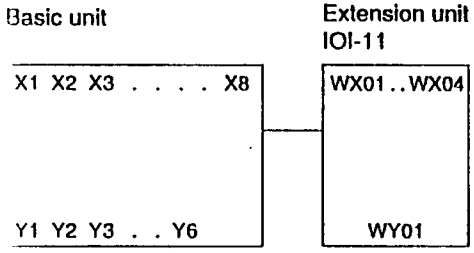
Addressing of the SESTEP 190

The control device consists of a basic unit with combined sink/source inputs and relay outputs and one digital and one analogue extension unit.

Addressing of the basic unit with one digital extension unit IOD-10
The basic unit uses 8 input addresses and 8 output addresses, but only the first six of the output addresses are used physically. The remaining two outputs can be used as internal registers. The addresses of the inputs and outputs of the digital extension unit start at address 9.



Addressing of the basic unit with one analogue extension unit IOI-11
The basic unit uses 8 input addresses and 8 output addresses. The analogue extension unit is activated with the internal register C0260. Then it uses the first four input registers WX01...WX04 (4 analogue inputs) and the first output register WY01 (1 analogue output).



Addressing of the SESTEP 290

The controller is able to distinguish between digital and analogue input modules, output modules and mixed I/O modules. These can be inserted in the racks in any desired sequence.

Addressing of the digital input and output modules
Digital input and output modules use 8 input addresses or 8 output addresses for each module. Mixed modules occupy 8 input and 8 output addresses, but only the lower four addresses of each are used physically. The remaining four inputs or outputs can be used as internal registers.

PCU-21	IDA-23	IDD-22	ODS-21	ODT-21	IOD-22	ODR-21
⋮	X001	X009	Y001	Y009	X017	Y025
sprecher+ schuh	•	•	•	•	•	•
	•	•	•	•	•	•
	•	•	•	•	X020	•
	•	•	•	•	Y017	•
	•	•	•	•	•	•
	•	•	•	•	•	•
SESTEP 290	X008	X016	Y008	Y016	Y020	Y032

The addresses X001...X008 are assigned to the first input module. The addresses X009...X016 are assigned to the next input module found. It is irrelevant whether this module is adjacent to the first input module in the rack, or whether there is one or more output modules between them.
The same definition is valid for the addressing of the output modules.

Addressing of the analogue input and output modules
Analogue input modules occupy 8 input addresses and 8 output addresses for each module. The desired channel is selected by the first two output addresses.
Analogue output modules occupy 16 output addresses for each module. The first output channel is addressed with the lower 8 addresses. The second channel is addressed with the higher 8 addresses.

PCU-21	IDD-22	IAU-22	ODR-21	OAU-22	ODT-21	IDA-23
⋮	X001	X009	Y009	Y017	Y033	X017
sprecher+ schuh	•	•	•	•	•	•
	•	•	•	•	•	•
	•	X016	•	Y024	•	•
	•	Y001	•	Y025	•	•
	•	•	•	•	•	•
	•	•	•	•	•	•
SESTEP 290	X008	Y008	Y016	Y032	Y040	X024

Analogue input channel:

Channel	Y 8n+1	Y 8n+2
1	OFF	OFF
2	ON	OFF
3	OFF	ON
4	ON	ON

C0253 If this special internal register is ON, it indicates that the preceding Process Reset was triggered by a power failure. The special internal register must be reset by forcing it to 0.

C0254 Reserved

C0255 RUN flag.
In operating mode RUN the internal register is ON. If a user program is copied into the external storage module in RUN mode, the status of the RUN internal register will be saved with it. If an EEPROM which has its RUN internal register set is used in the CPU, this will automatically be started. So it must not be started with a programming device.

C0256 Password flag. ON: Password exists OFF: No password

C0257* Reserved

C0258* Initialization flag
The special internal register is ON during the first program scan, from the second program scan on the internal register is OFF.

C0259* If the special internal register is ON, the forced elements will not be executed (except C0233...C0264). This reduces the program scan time.

The following special internal registers can be set and reset by the user program.

C0260* If the special internal register is ON, the access to the analogue extension module of the SESTEP 190 is possible.

C0261* Selection of the high-speed counter (HSCNT).
OFF: single-phase counter ON: 2 phase counter (S190)

C0262* Select direction of the high-speed counter (HSCNT).
C0261 = OFF, C0262 = OFF: incremental counter
C0261 = OFF, C0262 = ON: decremental counter

C0263* Write protection flag
Internal register = OFF: The clock registers are write protected.
Internal register = ON: The clock registers can be set.

C0264* Comparator signal of the high-speed counter

counter direction:	increment C0262 = OFF	decrement C0262 = ON
V0065 > V0161	ON	OFF
V0065 < V0161	OFF	ON
V0065 = V0161	ON	ON

These special internal registers cannot be used with the CPU module PCU-20 of the SESTEP 290.

Functions of the Special Registers

V0129 Average processing time (in units of 0.1 ms) for the last 64 runs through the program.

V0130 Number of input modules plugged in.

V0131 Number of output modules plugged in.

V0132* Address, where happened an error in the user program.

V0133 Reserved

V0134* Address, where the user program contains an element outside of the valid range.

V0135 Number of mains power failure. The register is cleared when the program memory area is cleared.

V0136 Operating mode of the CPU: 1 = STOP, 2 = RUN, 4 = Error

V0137 Reserved

V0138 Version number of the system program in the controller (BCD form).
i. e. 0314H: "03"=SESTEP 190, "14"=Version 1.4
"01"=S290 (PCU-20), "02"=S290 (PCU-21), "03"=S190

V0139 Count of the incorrect password keyin.

V0140* First element of the monitor area

V0141* Second element of the monitor area

V0142* Third element of the monitor area

V0143* Fourth element of the monitor area

V0144* Reserved

V0145* Retentive area of output Yxxx

V0146* Retentive area of internal register Cxxxx

V0147* Reserved

V0148* Reserved

V0149* Week-day (1=Monday, 7=Sunday)

V0150* Hour

V0151* Minute

V0152* Second

V0153* Year

V0154* Month

V0155* Day

V0156* Rest of a division

V0157*...

V0160* Timer with 0.01 s time base

V0161* Preset register of the high-speed counter

V0162*...

V0256* Reserved

* These special registers cannot be used with the CPU module PCU-20 of the SESTEP 290.