R.T.
YILDIZ TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

EVOLUTIONARY ALGORITHM BASED ELECTRONIC CIRCUIT DESIGN AUTOMATION

UFUK BOZKURT

MSc. THESIS
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This thesis which is prepared by Ufuk BOZKURT accepted as MSc thesis in YILDIZ TECHNICAL UNIVERSITY, Graduate School of Natural and Applied Sciences, Department of Electronics and Communication Engineering by the committee below on the date 29.06.2012.

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PREFACE

This master thesis was written while I was working in a network company named NETAS, therefore I was working at daytime and studying at nights for the thesis. It was a challenging and tiring task for me to be successful at work and successful at university. But I can not say that this is all done by myself. Therefore I would like to thank Dr. Revna Acar Vural and my supervisor Prof. Dr. Tülay Yıldırım for their guidances and great support. Without them, it was nearly impossible to complete this thesis.

Also I would like to express my deepest gratitudes to my family; my parents Medine and Hıdır Bozkurt, my brothers Hüseyin and Mustafa Bozkurt. During 3 years spending at work and at university, I couldn't share my time with them so much. But they always supported and helped me in every stage of my study as every stage of my life. From now on, they will see their little son and their little brother more than ever.

Finally, I dedicated this thesis to my 5 months old nephew Rüzgar Efe Bozkurt who doesn't recognize his uncle yet. I hope he will be a good engineer to make the people to overcome every obstacle and add a good value to humanity and then to Turkey.

May, 2012

Ufuk BOZKURT

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LIST OF SYMBOLS

A_V	Gain
C	Capacitor
C_{ox}	Oxide capacitance per unit area
CF	Cost function
CP	Crossover probability
C_R	Crossover constant
D	Dimension size
f_{-3dB}	Cut-off frequency
f_t	Unity-gain frequency
G	Generation
g_m	Transconductance of MOSFET
I_{bias}	Bias current
L	Gate length of MOSFET
η_j	Uniformly distributed random number within [0,1] of the j^{th} feature
$P^{(G)}$	Population over G. generation
Q	Quality factor
R	Resistor
τ_p	Propagation delay time
V_{tn}	Threshold voltage for NMOS
V_{tp}	Threshold voltage for PMOS
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
v_{IC}	Common-mode input voltage
v_{ID}	Differential-mode input voltage
V_{OS}	Input offset voltage
V_{DD}	Positive DC supply voltage
V_{SS}	Negative DC supply voltage
W	Gate width of MOSFET
ω	Angular frequency
$X_i^{(G)}$	j^{th} vector including feature of G^{th} population
(X_i')	j^{th} mutant vector including feature
λ	Channel-length modulation parameter

LIST OF ABBREVIATONS

ABC	Artificial Bee Colony
AIA	Artificial Immune Algorithm
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CSA	Clonal Selection Algorithm
DE	Differential Evolution
EA	Evolutionary Algorithm
FET	Field Effect Transistor
GA	Genetic Algorithm
GP	Genetic Programming
HM	Harmony Memory
HMCR	Harmony Memory Considering Rate
HMS	Harmony Memory Size
HS	Harmony Search
IC	Integrated Circuit
ICMR	Input Common Mode Range
MOS	Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
NP	Number of population
PAR	Pitch Adjust Rate
PSO	Particle Swarm Optimization
PMOS	P-channel Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
SA	Simulated Annealing
SPICE	Simulation Program with Integrated Circuit Emphasis
SR	Slew Rate
SVF	State Variable Filter
TS	Tabu Search
TSMC	Taiwan Semiconductor Manufacturing Company
VCVS	Voltage Controlled Voltage Source
VLSI	Very Large Scale Integration

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ABSTRACT

EVOLUTIONARY ALGORITHM BASED ELECTRONIC CIRCUIT DESIGN AUTOMATION

Ufuk BOZKURT

Department of Electronics and Communications Engineering

MSc. Thesis

Supervisor: Prof. Dr. Tülay YILDIRIM

Together with the increase in electronic circuit complexity, the design and optimization processes have to be automated with high accuracy. Generally, optimization is a very difficult and time consuming task including many conflicting criteria and a wide range of design parameters. Therefore, fast and accurate evolutionary methods are being utilized for accommodating required functionalities and performance specifications in electronic circuit design automation area.

Harmony Search and Differential Evolution algorithms are utilized for fast and optimal design of analog discrete and integrated circuit design having a fixed topology for a particular process technology. Simulation results indicate that these algorithms are very efficient methods for optimal component selection and sizing task in electronic circuit design automation. Since once programmed, no human intervention is required, the proposed method yields completely automated sizing of optimal circuits by means of both discrete and integrated design concepts.

Keywords: Harmony Search, Differential Evolution, Multi-objective Optimization, Design Automation.

ÖZET

EVRİMSEL ALGORİTMA TABANLI ELEKTRONİK DEVRE TASARIM OTOMASYONU

Ufuk BOZKURT

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Yüksek Lisans Tezi

Tez Danışmanı: Prof. Dr. Tülay YILDIRIM

Elektronik devrelerin karmaşıklığının artmasıyla, tasarım ve optimizasyon işlemlerinin de yüksek doğruluk ve yüksek hızda olması gerekliliği artmıştır. Genel olarak optimizasyon, devredeki bir çok kriter ve geniş bir dizayn parametresi sebebiyle oldukça zor ve zaman alan bir süreçtir. Bu sebeple elektronik devre tasarım otomasyonu, devrenin gerekli fonksiyonlarını ve performans kriterlerini yerine getirmesinde ve hızlı ve doğru evrimsel algoritmalara ihtiyaç duymuştur.

Harmoni Arama ve Farksal Gelişim algoritmaları, analog ayrık ve entegre devre tasarımında, hızlı ve en uygun yöntem olarak önerilmiştir. Simülasyon sonuçları, elektronik devre tasarım otomasyonunda optimum eleman seçimi ve boyutlandırma işi için bu algoritmaları etkin bir yöntem olarak göstermiştir. Bir kez programlandıktan sonra kullanıcı müdahalesi gerekmediğinden önerilen yöntem, devrelerin tamamen otomatik olarak boyutlandırmasını sağlamaktadır.

Anahtar Kelimeler: Harmoni Arama, Farksal Gelişim, Çok amaçlı Optimizasyon, Tasarım Otomasyonu.

YILDIZ TEKNİK ÜNİVERSİTESİ FEN BİLİMLERİ ENSTİTÜSÜ

CHAPTER 1

INTRODUCTION

1.1 Review of the Literature

Circuit design process can cover systems from the individual transistors to the complex electronic systems. This process begins with determining the specification which is the functionality that the design must provide, but does not indicate how it is to be done [1]. First step of the circuit design is to determine technical description of what the requirements are. These requirements can include a variety of electrical requirements and some of the physical parameters that design must meet. A designer first initiates the circuit design by determining a circuit topology by modifying a known topology instead of creating a new one. Next, the designer determines the values of parameters of a selected topology, such as transistor sizes and component values, to satisfy given specifications. Early in this stage, the designer may use analytical equations and assign approximate values to the design parameters. Later these values are refined by a circuit simulator such as SPICE after to check whether circuit satisfies design requirements or not [2].

Parameters $p=(x,s)$ which express the behavior of electronic circuits must be taken into account when optimizing performance functions $f(p)$; design parameters x and manufacturing process parameters s. During optimization, performance function $f(p)$ should be minimized, also several constraints must be satisfied [3]. Optimization is extensively used in following electronic design areas [4].

- Design accommodating complex device models

- Design accommodating non-standard specification constraints (minimum component spread, minimum sensitivity to component variations, maximum yield, etc.)
- Large-scale analog and digital circuit design; printed circuit board and interconnection; integrated circuit (IC) design and layout (e.g., minimum interconnection length, optimum placement of major functional blocks)
- Distributed device design (microwave, surface acoustic waveform structures, etc.)
- Passive component and topology selection in analog and digital filter design
- Neural network training for applications in electronic engineering

It is clear that the optimization complexity has increased in parallel with the increase of the circuit complexity of today's ICs. Thus finding the optimal solution meeting the criteria by hand became more unaffordable and time consuming. Besides, dramatic growth of search space makes the manual search process of the optimal solution inefficient. Therefore efficient optimization methods are required.

Classical approaches are either deterministic or statistical-based techniques. Deterministic methods, such as Simplex [5], Branch and Bound [6], Goal Programming [7], Dynamic Programming [8] are effective only for small size problems. They are not efficient when dealing with multi-criteria problems. Besides they do not offer general solution strategies. Most of the optimization problems require different types of variables, objective and constraint functions simultaneously in their formulation. Therefore, classic optimization procedures are generally not adequate. Heuristics are necessary to solve big size problems and/or with many criteria [9]. They can be easily modified and adapted to meet specific problem requirements. Even though they don't guarantee to find in an exact way the optimal solutions, they give good approximation of them within an acceptable computing time [10]. Some mathematical heuristics that were previously utilized were Local Search [11], Simulated Annealing (SA) [12], Tabu Search (TS) [13], Genetic Algorithms (GA) [14], Differential Evolution Algorithm (DE)[15], Harmony Search (HS) [16], [17] etc.

The application of nature inspired heuristics which is mentioned above in analog design automation and optimization is a promising area which is based on concepts of natural selection and survival of the fittest.

In [18], a comparative study on analog passive filter design with evolutionary methodologies was presented. An automated passive analog circuit synthesis procedure based on GA [19], genetic programming (GP) [20] and GP based tree representation method [21] was utilized for the simultaneous generation of both the topology and the component value selection. An evolutionary strategy method is presented in [22] where unconstrained and constrained evolutions were applied to analog low pass filter design. In [23], GP was used to evolve robust low-pass and high-pass analog passive filters. In [24], a GA based growing technique for component value optimization of analog passive filters was presented. Sheta [25] explored the advantages of DE over numerical optimization approaches to perform the selection of the best values of circuit elements for various types of band-pass filters. In [26] and [27] component value selection and topology optimization of analog active filter has been performed using GA and adaptive immune GA, respectively. Moreover, some particular analog active filter types were also optimized using evolutionary approaches in the literature. A voltage controlled voltage source (VCVS) low pass Butterworth active filter circuit was designed using clonal selection algorithm (CSA) and results of CSA based design was compared with results of TS, GA and conventional design methods [28]. Particle swarm optimization (PSO) and artificial bee colony (ABC) based component value selection methods [29], [30] have been utilized for the optimal design of the same circuit topology used in [28] and less design error [29], [30] was obtained when compared with results of [28]. In [30], [31], [32], [33] and [34], component values of a low pass state variable active filter (SVF) circuit was determined using ABC, PSO, GA, TS and artificial immune algorithm (AIA), respectively.

1.2 Aim of the Thesis

In this study, the applicability of nature inspired metaheuristics in analog active filter design is investigated by means of both accuracy and elapsed time. Two analog active filter topologies, 4th order VCVS Butterworth filter [28], [29], [30] and a 2nd order low

pass SVF [30], [31], [35], are designed using DE and HS algorithm. SVF filter is designed using discrete components selected from two different manufactured series in order to investigate the performance of DE and HS when tighter tolerances are preferred in discrete component selection.

Another problem considered in this work is the optimal selection of transistor dimensions of CMOS differential amplifier, CMOS operational amplifier and CMOS comparator for minimum occupied MOS transistor area. Here, particular specifications for a specified topology of these ICs are aimed to be met by adjusting design variables such as device sizes and bias current with two nature-inspired metaheuristics, DE and HS. Metaheuristics are introduced to obtain near-optimal solutions for a given cost function (CF) in a reasonable amount of computation time. The most recognized works on metaheuristic based analog IC sizing are investigated in [36] and [37]. Developed by Storn and Price, DE is one of the most widely used metaheuristics for analog IC sizing [38], [39], [40], [41], [42], [43], [44], [45]. A more recently introduced metaheuristic technique, HS has only been investigated in [45] for sizing of CMOS operational transconductance amplifier. To see whether DE and HS algorithms are useful for automation of circuit optimization, we compared the results with another algorithms which are studied previously in [2].

1.3 Hypothesis

With this study, we will provide that evolutionary algorithms are useful for electronic circuit design automation. With these algorithms; the time spent on circuit design will be reduced dramatically. The organization of this dissertation is as follows: Chapter 2 provides an insight of the evolutionary techniques. Chapter 3 provides selections of passive components of two different analog active filter structures for two different manufactured series. Results are discussed in detail. Chapter 4 describes design equations of differential amplifier with current mirror load source, two-stage operational amplifier and comparator. Also the methods for optimal sizing of MOS transistors for minimum occupied area are provided. Results are discussed in detail. Chapter 5 concludes with a discussion of simulation results and suggests possible extensions.

CHAPTER 2

EVOLUTIONARY ALGORITHMS

Evolutionary algorithm (EA) is a subset of evolutionary computation which refers to computer-based problem solving systems that use computational models of evolutionary processes. Each EA maintains a population of candidate solutions. One of the canditate solutions to the optimization problem are chosen by the fitness function of the EA as the optimal solution of that problem at the end of the optimization process. In order to terminate the optimization process, one of the following conditions should be satisfied.

- A specified number of generations or iterations have been exceeded.
- There is no improvement in optimal solution over a number of generations.
- An acceptable solution is found.

2.1 Harmony Search Algorithm

Harmony Search (HS) is a music-based metaheuristic optimization algorithm. It was inspired by the observation that the aim of music is to search for a perfect state of harmony. Scientists have found such an interesting connection by developing a new algorithm, called Harmony Search. HS was first developed by Geem et al. in 2001 [16]. Since its first appearance in 2001, it has been applied to many optimization problems including function optimization, engineering optimization, design of water distribution networks, groundwater modeling, energy-saving dispatch, truss design, vehicle routing, and others [46], [47].

The effort to find the harmony in music is to find the optimality in an optimization process. In other words, a jazz musician's improvisation process can be compared to the search process in optimization. On one hand, the perfectly pleasing harmony is determined by the audio aesthetic standard. A musician always intends to produce a piece of music with perfect harmony. On the other hand, an optimal solution to an optimization problem should be the best solution available to the problem under the given objectives and limited by constraints. Both processes intend to produce the best or optimum [48]. Following figure is the steps of HS algorithm.

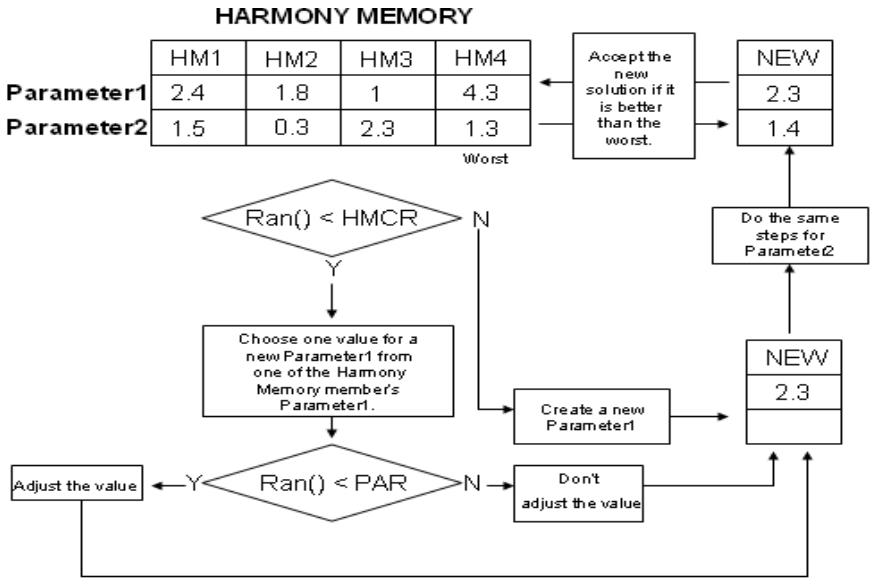

Figure 2. 1 Steps of HS algorithm

The total number of individual solutions to the optimization problem is equal to harmony memory size (HMS) and individuals are stored in harmony memory (HM). Following, a new solution is improvised according to harmony memory considering rate (HMCR). A stored value is chosen from HM with probability of HMCR ($0 \leq HMCR \leq 1$) and 1-HMCR is the probability of generating it randomly. If the solution is picked from HM, it is mutated according to the pitch adjust rate ($0 \leq PAR \leq 1$). After HM is updated the fitness values are evaluated. If the improvised solution yields a better fitness than that of the worst member in HM, it replaces the worst one. Otherwise the improvised one is eliminated. The above procedure is repeated until a preset termination criterion (maximum iterations or a target fitness value) is met [16].

2.2 Differential Evolutionary Algorithm

Differential Evolution (DE) is a real coded population-based optimization technique based on parallel direct search method and developed by Storn and Price [15]. It diverges from Genetic Algorithm (GA) by adding the weighted difference between two chromosomes to the third in order to generate new ones. DE uses a population *P* having *NP* individuals that evolves over *G* generations to reach the optimal solution. Each individual X_i is a vector that features a dimension size of *D*.

$$P^{(G)} = [X_1^{(G)}, \ldots, X_{NP}^{(G)}]^T \tag{2.1}$$

$$X_i^{(G)} = [X_{i,1}^{(G)}, \ldots, X_{i,D}^{(G)}],\ i= 1,\ldots,NP \tag{2.2}$$

Algorithm starts by creating an initial population of *NP* vectors. Each vector in population matrix is assigned follows.

$$X_j=X_j^{min}+\eta_j(X_j^{max}-X_j^{min}),\ j= 1,\ldots,D \tag{2.3}$$

Where X_j^{max}, X_j^{min} are the upper, lower bounds, respectively and η_j is a uniformly distributed random number within [0,1] of the j^{th} feature. The optimization process in DE is carried out using the three basic operation; mutation, crossover and selection. The mutation operator generates mutant vectors (X_i') according to (2.4).

$$X_i'^{(G)} = X_a^{(G)}+F(X_b^{(G)} – X_c^{(G)}),\ a\neq b\neq c\neq i \tag{2.4}$$

Where X_a, X_b and X_c are randomly selected vectors among population matrix including *NP* different vectors. *F* is the scaling constant used to improve algorithm convergence. The crossover operation is employed to create trial vectors (X_i'') by mixing the individuals of the mutant vectors (X_i') with the target vector (X_i) according to (2.5).

$$X_{i,j}^{''(G)} = \begin{cases} X_{i,j}^{'(G)}, if\ (\eta_j' \leq C_R) or (j = q) \\ X_{i,j}^{(G)}, otherwise \end{cases} \tag{2.5}$$

Where *q* is a randomly chosen index within [1,*NP*], guaranteeing that trail vector employs at least one individual from the mutant vector. C_R is the crossover constant within [0,1] that controls the population diversity. Finally selection operator compares the fitness values of trial vectors and target vectors. If trial vectors yield better fitness values then they replace the target vectors with which they were compared, otherwise

predetermined population member is retained. The above procedure restarts until the chromosomes have been successfully updated to improve their fitness values to a specified value [15], [49].

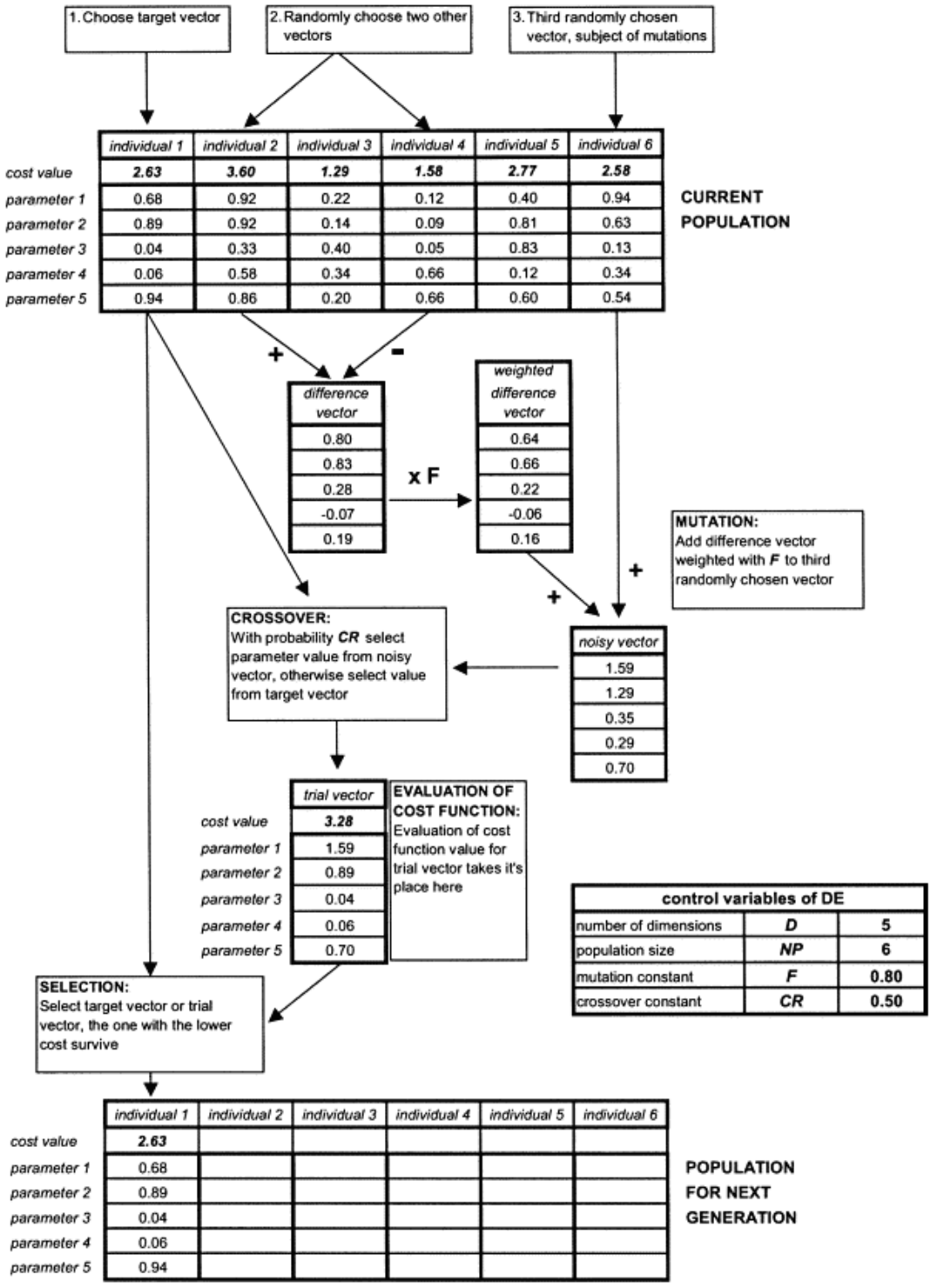

Figure 2. 2 Steps of DE for the function $F(x) = x_1 + x_2 + x_3 + x_4 + x_5$ [50]

CHAPTER 3

EVOLUTIONARY ALGORITHMS FOR ANALOG DISCRETE CIRCUIT DESIGN

In order to investigate the usage of nature inspired metaheuristics in active filter design and to compare with previous methods, two different low-pass analog active filter circuits are selected. Design problem has been introduced by composing an equation consists of design parameters, as CF. In the beginning of the algorithm, a certain range was determined for design parameters by human designer. DE and HS should minimize the given CF and obtain design criteria and design parameter values for the specified range which gives minimum CF value. In this study, the aim is to estimate the preferred values of resistors and capacitors of the selected circuit with minimum design error [30], [32], [51].

3.1 EA Based Butterworth Filter Design

In following sub-sections Butterworth filter structure was examined and the required equations were determined. Then DE and HS algorithms were used to find the optimal solution for the required equations. As a last step results were compared with previous methods.

3.1.1 Butterworth Filter Structure

Butterworth filters are termed maximally-flat-magnitude-response filters, optimized for gain flatness in the pass-band. The 4^{th} order VCVS low-pass Butterworth filter can be realized by cascading two second order blocks as depicted in Figure 3.1.

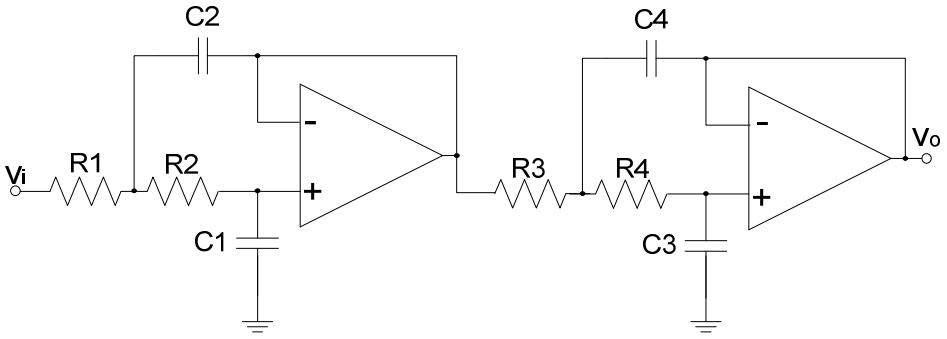

Figure 3. 1 Butterworth 4th order VCVS low-pass filter topology [28], [29] ,[30]

The response of a 4th order Butterworth low pass filter is specified by cutoff frequency (ω_{c1}, ω_{c2}) and quality factor (Q_1, Q_2) of two second order filters are given in (3.1) and (3.2).

$$\omega_{c1} = \frac{1}{\sqrt{\mathrm{R}_1\mathrm{R}_2 C_1 \mathrm{C}_2}}, \omega_{c2} = \frac{1}{\sqrt{\mathrm{R}_3\mathrm{R}_4 C_3 \mathrm{C}_4}} \tag{3.1}$$

$$Q_1 = \frac{\sqrt{\mathrm{R}_1\mathrm{R}_2 C_1 \mathrm{C}_2}}{R_1 C_1 + R_2 C_1}, Q_2 = \frac{\sqrt{\mathrm{R}_3\mathrm{R}_4 C_3 \mathrm{C}_4}}{R_3 C_3 + R_4 C_3} \tag{3.2}$$

In order to make a true comparison with [28], [29] and [30], same error criterion is adopted. Design error of Butterworth filter (3.3) is the summation of cost function error of cutoff frequency ($CF_{\omega\text{-}BF}$) and quality factor ($CF_{Q\text{-}BF}$). Those definitions are provided in (3.4) where target cut-off frequency ω_c is 10k rad/s and target quality factors Q_{t1} and Q_{t2} are 1.3065 and 0.5412, respectively.

$$Error_{BF} = 0.5CF_{\omega-BF} + 0.5CF_{Q-BF} \tag{3.3}$$

$$CF_{\omega-BF} = \frac{\left|\omega_{c1} - \omega_c\right| + \left|\omega_{c2} - \omega_c\right|}{\omega_c}$$
$$CF_{Q-BF} = \frac{\left|Q_1 - Q_{t1}\right|}{Q_{t1}} + \frac{\left|Q_2 - Q_{t2}\right|}{Q_{t2}} \tag{3.4}$$

Total error definition of Butterworth filter is rewritten by means of design parameters (R1...4, C1...4) in (3.5). The right side of (3.5) would constitute the CF which DE and HS

algorithms would minimize. They should also obtain the preferred values of design parameters that minimize CF. In each decade, any of twelve preferred values can be taken according to standard E12 series within the range of 10^3 to 10^6 ohms for resistors and 10^{-9} to 10^{-6} farads for capacitors.

$$Error_{BF} = \left(\begin{array}{l} 0.5\dfrac{\left|\dfrac{1}{\sqrt{R_1R_2C_1C_2}} - \omega_c\right| + \left|\dfrac{1}{\sqrt{R_3R_4C_3C_4}} - \omega_c\right|}{\omega_c} \\ + 0.5\dfrac{\left|\dfrac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1} - 1.3065\right|}{1.3065} + 0.5\dfrac{\left|\dfrac{\sqrt{R_3R_4C_3C_4}}{R_3C_3 + R_4C_3} - 0.5412\right|}{0.5412} \end{array} \right) \quad (3.5)$$

The number of capacitors and resistors constitute the feature size of an individual in the population matrix of both DE and HS methods. Since the probable values vary from three decade range, a coding scheme is used as in (3.6).

$R_1 = a \times 100 \times 10^{a1}\ (\Omega)$, $R_2 = b \times 100 \times 10^{b1}\ (\Omega)$

$R_3 = c \times 100 \times 10^{c1}\ (\Omega)$, $R_4 = d \times 100 \times 10^{d1}\ (\Omega)$ (3.6)

$C_1 = e \times 100 \times 10^{e1}\ (pF)$, $C_2 = f \times 100 \times 10^{f1}\ (pF)$

$C_3 = g \times 100 \times 10^{g1}\ (pF)$, $C_4 = h \times 100 \times 10^{h1}\ (pF)$

Since each resistor should take an E12 serial value in the range of 10^3 to 10^6 ohms, the design constraint for resistors given in (3.7) must be satisfied. Similarly each capacitor should take E12 serial value in the range of 10^{-9} to 10^{-6} farads. If capacitor values are defined in picofarads (pF) then design constraint for capacitors given in (3.8) would be valid.

$$0.1 \le a, b, c, d \le 0.82 \quad 2 \le a1, b1, c1, d1 \le 4 \quad (3.7)$$

$$0.1 \le e, f, g, h \le 0.82 \quad 2 \le e1, f1, g1, h1 \le 4 \quad (3.8)$$

3.1.2 Simulation Results

Butterworth filter components are selected from E12 series with a target CF value aimed to be smaller than 0.007. Considering DE method, this requirement has been met at the 36544th iteration in 45.68 s and the exact CF value is obtained as 0.0057 with crossover probability (CR) of 0.3, scaling constant (F) of 1.5, and individuals in the population (NP) is 12. The effect of DE's own parameters over design error values (CF values) is given in Table 3.1. 0.0066 has been obtained as design error with HS optimization at the 15000th iteration in 5.2 s with a memory size (HMS) of 10, considering rate (HMCR) of 0.9 and a pitch adjust rate between 0.1 and 0.9. The effect of HS's own parameters over CF values is tabulated in Table 3.2.

Following, we explored the performance of nature-inspired metaheuristics over 20 runs with optimal own parameters as given in Table 3.1 and Table 3.2. The resulting CF values obtained in each run were used to produce box and whisker plots to show the median performance of DE and HS as given in Figure 3.2. Upper and lower ends of boxes represent 75th and 25th percentiles. Median is depicted by the red line. The whiskers are lines extending from each end of the boxes to show the extent of the rest of the data.

Simulations are performed in MATLAB environment with Intel Core 2 Duo CPU, T7300 @ 2.00GHz.

Table 3.1 Effects of DE own parameters on Butterworth filter design performance

CF Values (DE-E12)	*NP = 8*			***NP = 12***		
	CR = 0.3	*CR = 0.5*	*CR = 1*	***CR = 0.3***	*CR = 0.5*	*CR = 1*
F = 0.5	0.013	0.009	0.255	0.014	0.009	0.255
F = 1.0	0.007	0.022	0.582	0.008	0.009	0.062
F = 1.5	0.008	0.012	0.147	**0.0057**	0.007	0.013
F = 2.0	0.009	0.014	0.040	0.017	0.012	0.144

Table 3.2 Effects of HS own parameters on Butterworth filter design performance

CF Values (HS-E12)	*HMS = 5*			***HMS = 10***		
	HMCR = 0.3	*HMCR = 0.6*	*HMCR = 0.9*	*HMCR = 0.3*	*HMCR = 0.6*	***HMCR = 0.9***
PAR = 0.4- 0.9	0.051	0.045	0.013	0.119	0.013	0.019
PAR = 0.1- 0.9	0.11	0.052	0.007	0.118	0.028	**0.0066**
PAR = 0.1- 0.6	0.10	0.010	0.016	0.09	0.028	0.016

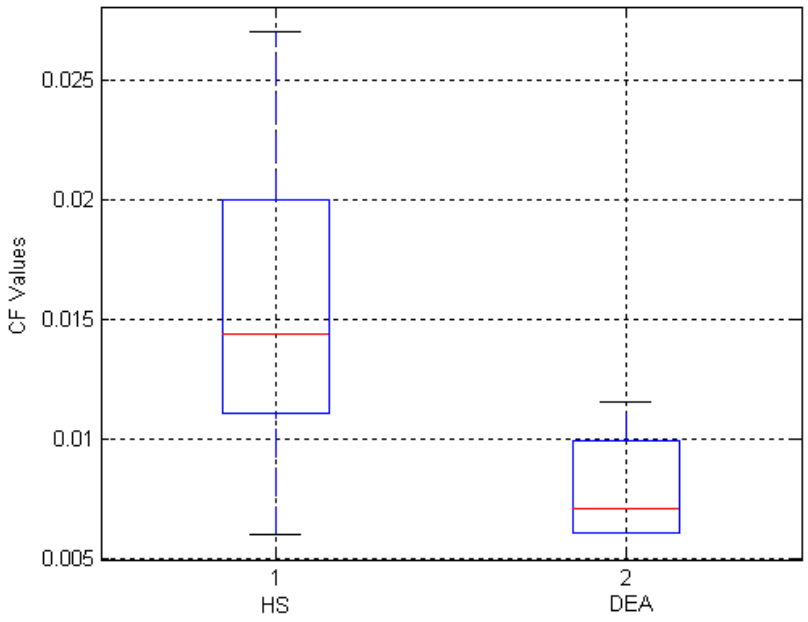

Figure 3.2 Box and whisker plots of DE and HS algorithms for Butterworth filter design with E12 series over 20 runs

CF values versus iteration number for five independent runs are plotted in Figure 3.3 and Figure 3.4 for DE and HS algorithms, respectively. In those figures, it can be seen that number of iterations required to achieve the quality requirements are slightly different in each run.

Exact values of discrete components, total error and computation time of DE and HS based design and previously used methods are tabulated in Table 3.3. Compared to the previous methods and other techniques, DE and HS algorithm achieved the smaller design errors among the other methods in a shorter computation time than GA and PSO.

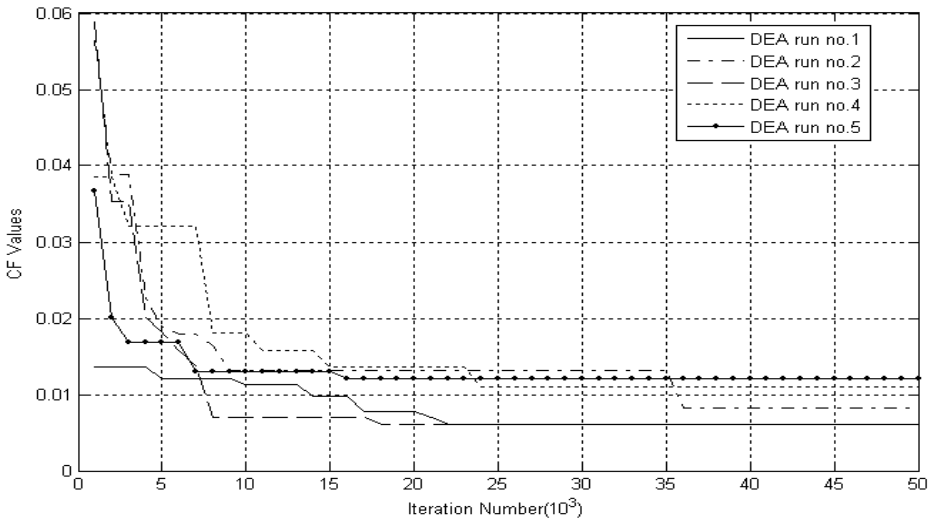

Figure 3.3 CF versus iteration number for DE algorithm (E12)

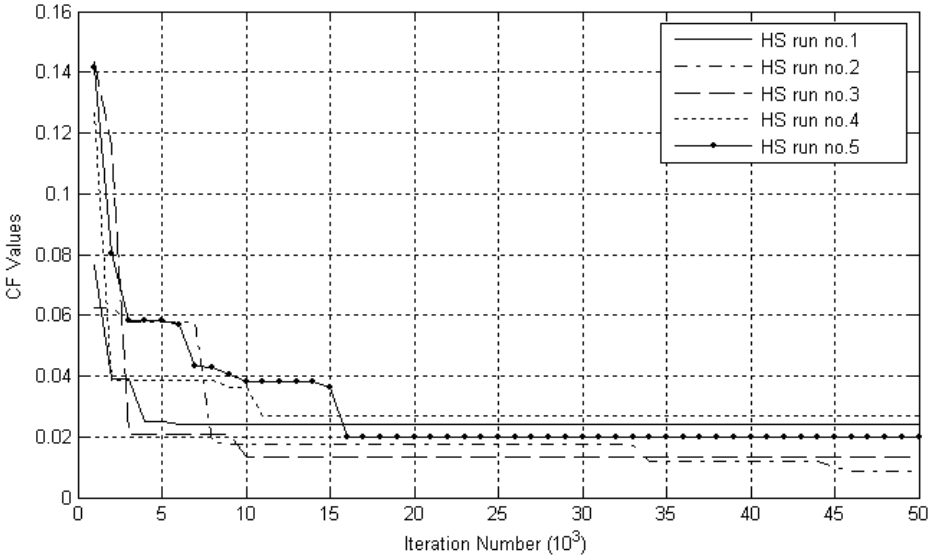

Figure 3.4 CF versus iteration number for HS algorithm (E12)

Following, we employed Monte Carlo analysis in order to investigate robustness of DE and HS based Butterworth Filter design in case of component value variations due to specified tolerances of manufactured series. One hundred different trials of Monte Carlo simulations were applied by adding tolerance value of relevant manufacturing series for each analog filter structure where AC simulation results for ten trials are depicted in Figure 3.5 and Figure 3.6. Tolerance values are randomly chosen from %0 up to %10 which is the maximum value for E12 series.

Table 3.3 Component values and performance of previous methods vs DE and HS algorithms for Butterworth filter design

	TS [28]	**GA [28]**	**CSA [28]**	**GA [30]**	**ABC [30]**	**PSO [29,30]**	**HS**	**DE**
R1(kΩ)	27	4.7	4.7	6.8	4.7	4.58	5.6	4.7
R2(kΩ)	0.27	1.8	4.7	6.8	4.7	4.7	5.6	4.7
C1(nF)	2.7	12	8.2	5.6	8.2	8.2	6.8	8.2
C2(nF)	470	100	56	39	56	56	47	56
R3(kΩ)	220	100	0.27	39	1	1.1	180	180
R4(kΩ)	0.82	4.7	27	1	39	1	5.6	5.6
C3(nF)	82	1.8	6.8	4.7	4.7	87.6	1	1
C4(nF)	0.68	12	200	56	56	102.2	10	10
Total Error	0.02778	0.01817	0.00789	0.0166	0.0113	0.0076	0.00667	**0.00573**
Time	-	-	-	4.1 min	0.7 s	3.2 min	5.2 s	45.68 s

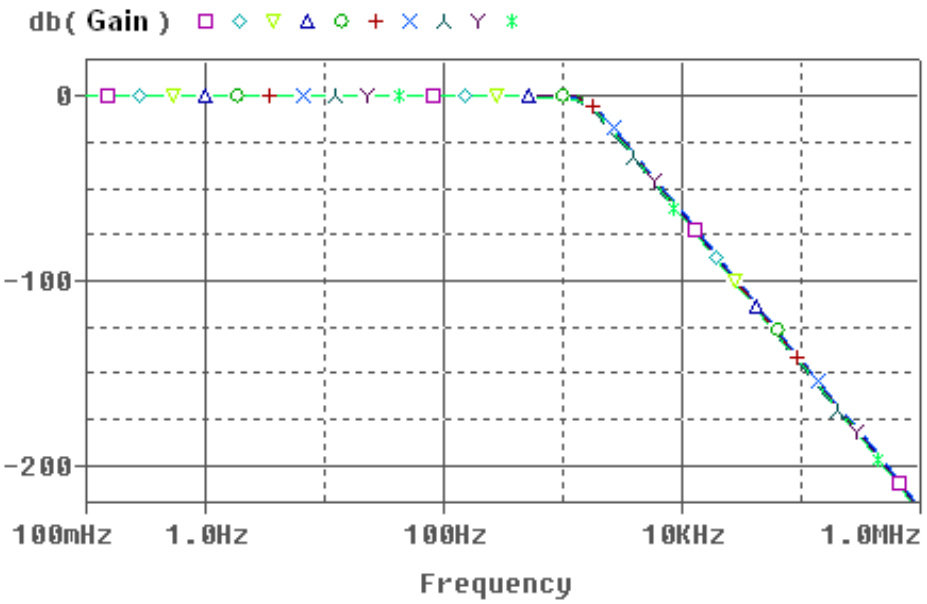

Figure 3.5 Monte Carlo analysis for DE based Butterworth filter design (E12)

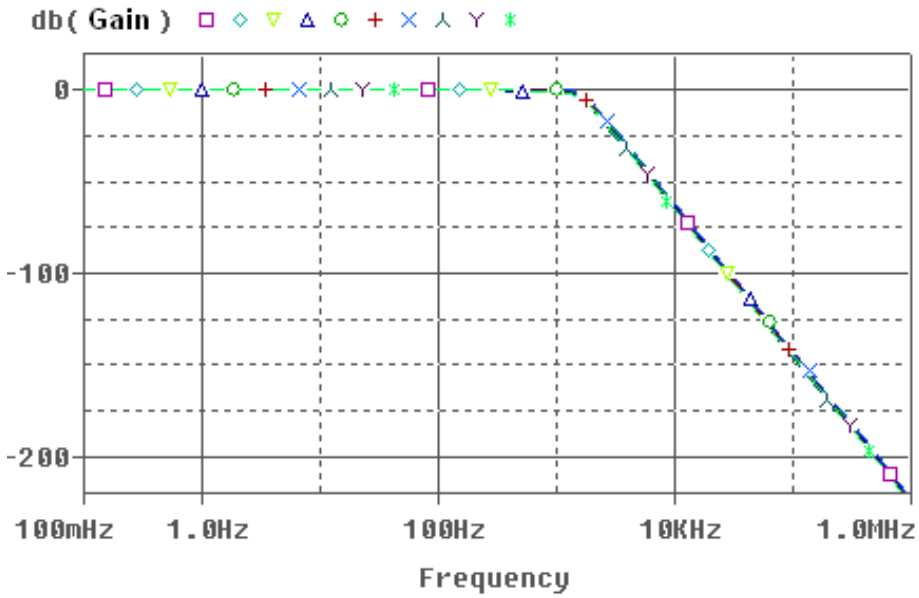

Figure 3.6 Monte Carlo analysis for HS based Butterworth filter design (E12)

3.2 EA Based State Variable Filter Design

In following sub-sections State Variable filter structure was examined and the required equations were determined. And then DE and HS algorithms were used to find the optimal solution for the required equations. As a last step results were compared with previous methods.

3.2.1 State Variable Filter Structure

A state variable filter (SVF) realizes the state-space model directly. The instantaneous output voltage of one of the integrators corresponds to one of the state-space model's state variables. A second-order SVF is illustrated in Figure 3.7 and is well described in [35]. The low pass output is assumed here to be the desired output.

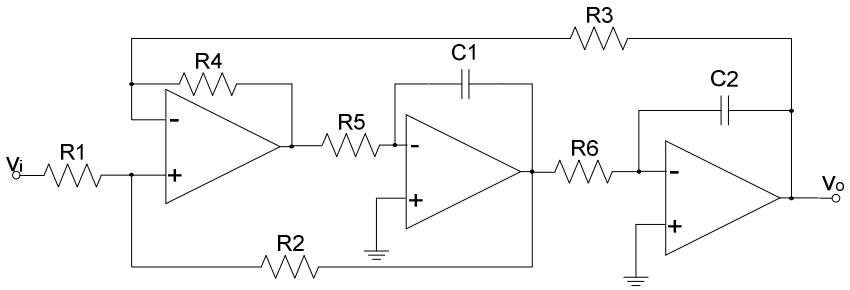

Figure 3.7 State variable 2nd order low pass filter topology [30], [31], [35]

The response of a 2nd order low pass SVF circuit is specified by the cut-off frequency ($\omega_{SVF}=2\pi f_{SVF}$) and the quality factor (Q_{SVF}) as given in (3.9).

$$\begin{aligned} \omega_{SVF} &= \sqrt{\left(\frac{R_4}{R_3}\right)\left(\frac{1}{C_1 C_2 R_5 R_6}\right)} \\ Q_{SVF} &= \frac{R_3(R_1+R_2)}{R_1(R_3+R_4)}\sqrt{\frac{C_1 R_4 R_5}{C_2 R_3 R_6}} \end{aligned} \tag{3.9}$$

In order to make a true comparison with [30] and [31], same error criterion is adopted. Design error of SVF (3.10) is the summation of cost function error of cutoff frequency ($CF_{\omega\text{-}SVF}$) and quality factor ($CF_{Q\text{-}SVF}$). Those definitions are provided in (3.11). The target cut-off frequency (ω_0) is 10k rad/s (f_{SVF}=10000/(2*π)=1591.55 Hz) and target quality factor (Q_t) is 0.707 for reduced peak on low pass response.

$$Error_{SVF} = 0.5CF_{\omega-SVF} + 0.5CF_{Q-SVF} \tag{3.10}$$

$$\begin{aligned} CF_{\omega-SVF} &= \frac{\left|\omega_{SVF}-\omega_0\right|}{\omega_0} \\ CF_{Q-BF} &= \frac{\left|Q_{SVF}-Q_t\right|}{Q_t} \end{aligned} \tag{3.11}$$

Total error definition of SVF is rewritten by means of design parameters ($R_{1\ldots6}$, $C_{1,2}$) in (3.12). The right side of (3.12) would constitute the CF which DE and HS would minimize. They should also obtain the preferred values of discrete components that minimize CF. In each decade, any of twenty four and ninety six preferred values can be taken according to E24 and E96 series, respectively within the range of 10^3 to 10^6 ohms for resistors and 10^{-9} to 10^{-6} farads for capacitors.

$$Error_{BF} = \left(\begin{array}{l} 0.5 \dfrac{\left| \sqrt{\dfrac{R_4}{R_3} \dfrac{1}{R_5 R_6 C_1 C_2}} - \omega_0 \right|}{\omega_0} \\ + 0.5 \dfrac{\left| \dfrac{R_3(R_1 + R_2)}{R_1(R_3 + R_4)} \dfrac{C_1 R_4 R_5}{C_2 R_3 R_6} - Q_t \right|}{Q_t} \end{array} \right) \quad (3.12)$$

The number of capacitors and resistors constitute the feature size of an individual in the population matrix of both DE and HS methods. Since the probable values vary from three decade range, a coding scheme is used as in (3.13)**.**

$$\begin{array}{l} R_1 = a \times 100 \times 10^{a1}\,(\Omega), \quad R_2 = b \times 100 \times 10^{b1}\,(\Omega) \\ R_3 = c \times 100 \times 10^{c1}\,(\Omega), \quad R_4 = d \times 100 \times 10^{d1}\,(\Omega) \\ R_5 = e \times 100 \times 10^{e1}\,(pF), \quad R_6 = f \times 100 \times 10^{f1}\,(pF) \\ C_1 = g \times 100 \times 10^{g1}\,(pF), \quad C_2 = h \times 100 \times 10^{h1}\,(pF) \end{array} \quad (3.13)$$

DE and HS estimated the component values of the SVF circuit for different preferred series. First, SVF is designed with components that are compatible with E24 series. Since each resistor should take an E24 serial value in the range of 10^3 to 10^6 ohms, the design constraint for resistors given in (3.14) must be satisfied. Similarly each capacitor should take E24 serial value in the range of 10^{-9} to 10^{-6} farads. If capacitor values are defined in picofarads (pF) then design constraint for capacitors given in (3.15) would be valid.

$$0.1 \le a, b, c, d, e, f \le 0.91 \qquad 2 \le a1, b1, c1, d1, e1, f1 \le 4 \quad (3.14)$$

$$0.1 \le g, h \le 0.91 \qquad 2 \le g1, h1 \le 4 \quad (3.15)$$

Following, DE and HS algorithm estimated the component values of SVF circuit that are compatible with E96 series. Design constraints are specified similarly as explained for E24 series. The difference is the upper limit constraints for resistors and capacitors s given in (3.16) and (3.17).

$$0.1 \le a, b, c, d, e, f \le 0.976 \qquad 2 \le a1, b1\ c1, d1, e1, f1 \le 4 \quad (3.16)$$

$$0.1 \le g, h \le 0.976 \qquad 2 \le g1, h1 \le 4 \quad (3.17)$$

3.2.2 Simulation Results

SVF components are selected from E24 and E96 series with a target CF value aimed to be smaller than $5x10^{-5}$. Considering E24 series, DE method met this requirement at the 34652^{th} iteration in 36.7 s and the exact CF value is obtained as $3.23x10^{-5}$ with crossover probability (C_R) of 0.3, scaling constant (F) of 0.5, and individuals in the population (NP) is 12. The effect of DE's own parameters over design error values (CF values) is given in Table 3.4. HS optimization could not reach target value within maximum iteration limit. However a CF value of $1.94x10^{-4}$ is obtained at 232138^{th} iteration in 79.8 s with a memory size (HMS) of 5, considering rate ($HMCR$) of 0.9 and a pitch adjust rate (PAR) between 0.4 and 0.9. The effect of HS's own parameters over CF values is tabulated in Table 3.5. The performance of nature-inspired metaheuristics is explored over 20 runs with optimal own parameters as given in Table 3.4 and Table 3.5. Simulations are performed in MATLAB environment with Intel Core 2 Duo CPU, T7300 @ 2.00GHz.

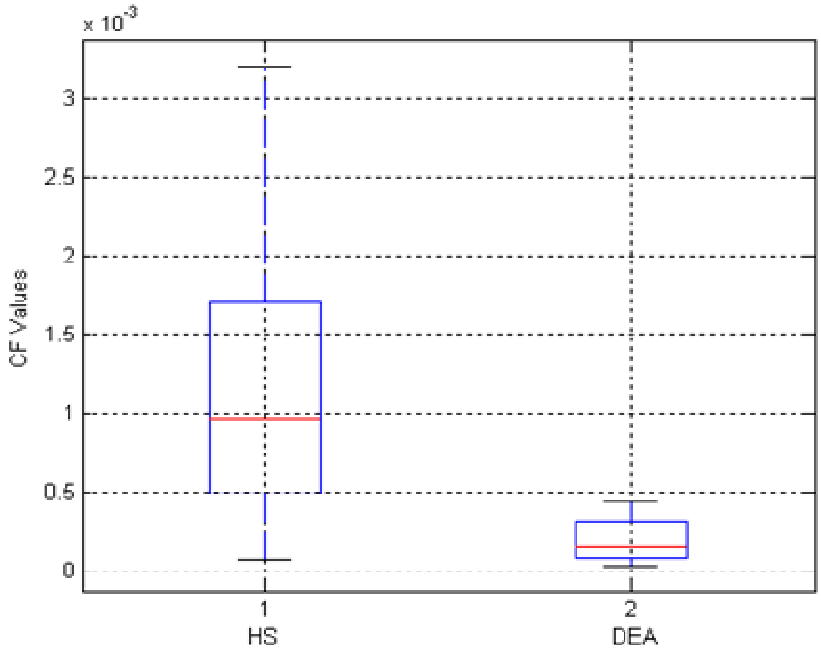

Figure 3.8 Box and whisker plots of DE and HS algorithms for SVF design with E24 series over 20 runs

The resulting CF values obtained in each run for SVF design with E24 series were used to produce box and whisker plots in Figure 3.8. CF values versus iteration number for five independent runs are plotted in Figure 3.9 and Figure 3.10 for DE and HS algorithms, respectively.

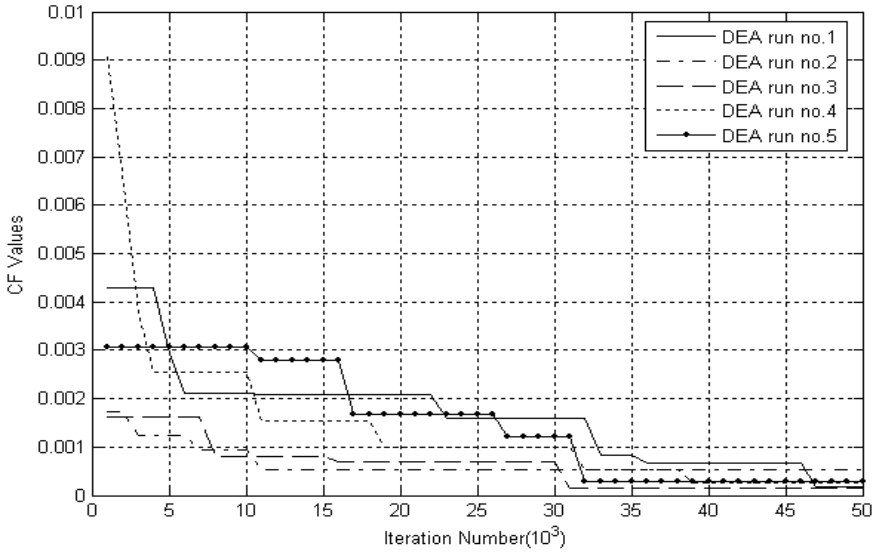

Figure 3.9 CF versus iteration number for DE algorithm (E24)

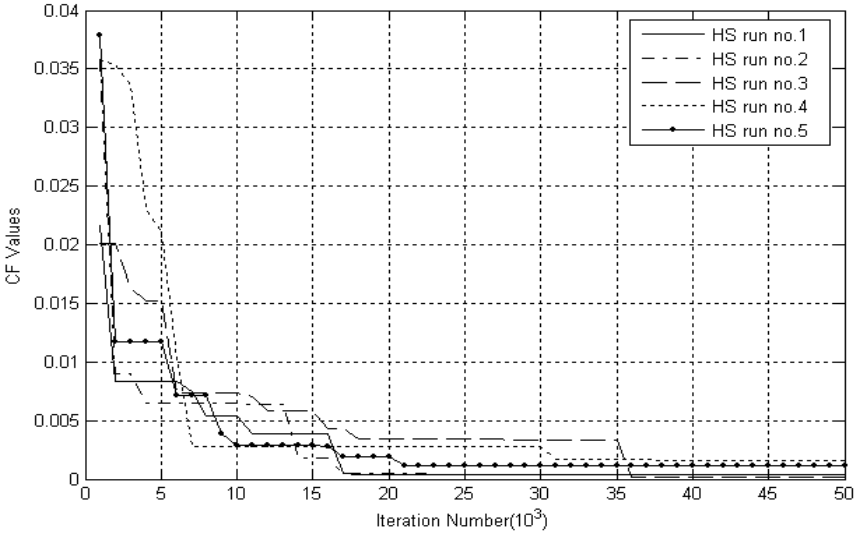

Figure 3.10 CF versus iteration number for HS algorithm (E24)

Table 3.4 Effects of DE own parameters on SVF design performance (E24)

CF Values (DE-E24)	*NP = 8*			***NP = 12***		
	CR = 0.3	*CR = 0.5*	*CR = 1*	***CR = 0.3***	*CR = 0.5*	*CR = 1*
F = 0.5	1.71×10^{-4}	2.00×10^{-4}	2.89×10^{-2}	$\mathbf{3.23 \times 10^{-5}}$	1.81×10^{-4}	4.8×10^{-3}
F = 1.0	9.67×10^{-5}	7.79×10^{-4}	4.03×10^{-2}	4.3×10^{-4}	5.34×10^{-4}	3.1×10^{-3}
F = 1.5	2.22×10^{-4}	9.19×10^{-4}	1.1×10^{-2}	5.74×10^{-4}	8.37×10^{-4}	2.31×10^{-4}
F = 2.0	6.57×10^{-4}	4.41×10^{-4}	2.87×10^{-2}	5.25×10^{-5}	1.90×10^{-4}	3.88×10^{-4}

Table 3.5 Effects of HS own parameters on SVF design performance (E24)

CF Values (HS-E24)	***HMS = 5***			*HMS = 10*		
	HMCR = 0.3	*HMCR = 0.6*	***HMCR = 0.9***	*HMCR = 0.3*	*HMCR = 0.6*	*HMCR = 0.9*
PAR = 0.4- 0.9	0.0014	9.05×10^{-4}	$\mathbf{1.94 \times 10^{-4}}$	0.0046	0.015	7.87×10^{-4}
PAR = 0.1- 0.9	0.0069	0.0020	5.29×10^{-4}	0.0018	0.014	2.75×10^{-4}
PAR = 0.1- 0.6	0.0043	0.0013	6.82×10^{-4}	0.0021	0.031	7.84×10^{-4}

Finally, components of SVF are selected from E96 series in order to investigate whether performance of DE and HS will be affected when same topology is designed with a tighter tolerance manufactured series. Target CF value for SVF design with E24 series is retained. A total design error of 1.95x10-5 is obtained with DE method at the 47169th iteration in 50 s with crossover probability (CR) of 0.5, scaling constant (F) of 0.5, and individuals in the population (NP) is 12. The effect of DE's own parameters over design error values (CF values) is given in Table 3.6. HS algorithm has successfully minimized total error in 102.8 s at 298725th iteration. CF value of 1.66x10-5 is obtained with a HMS of 5, HMCR of 0.9 and PAR between 0.4 and 0.9. The effect of HS's own parameters over CF values is tabulated in Table 3.7. The performance of nature-inspired metaheuristics is explored over 20 runs with optimal own parameters as given in Table 3.6 and Table 3.7. The resulting CF values obtained in each run for SVF design with E96 series were used to produce box and whisker plots as in Figure 3.11. CF values versus iteration number for five independent runs are plotted in Figure 3.12 and Figure 3.13 for DE and HS, respectively.

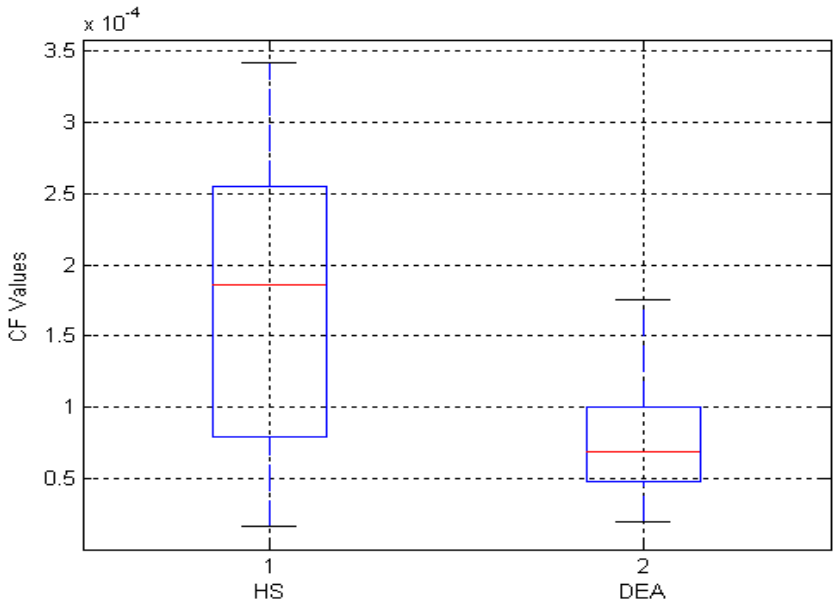

Figure 3.11 Box and whisker plots of DE and HS algorithms for SVF design with E96 series over 20 runs

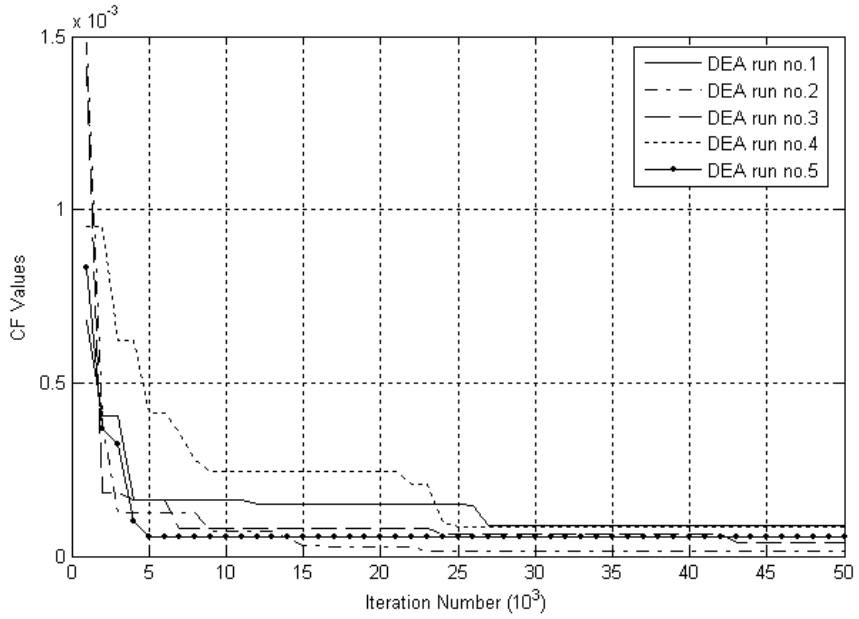

Figure 3.12 CF versus iteration number for DE algorithm (E96)

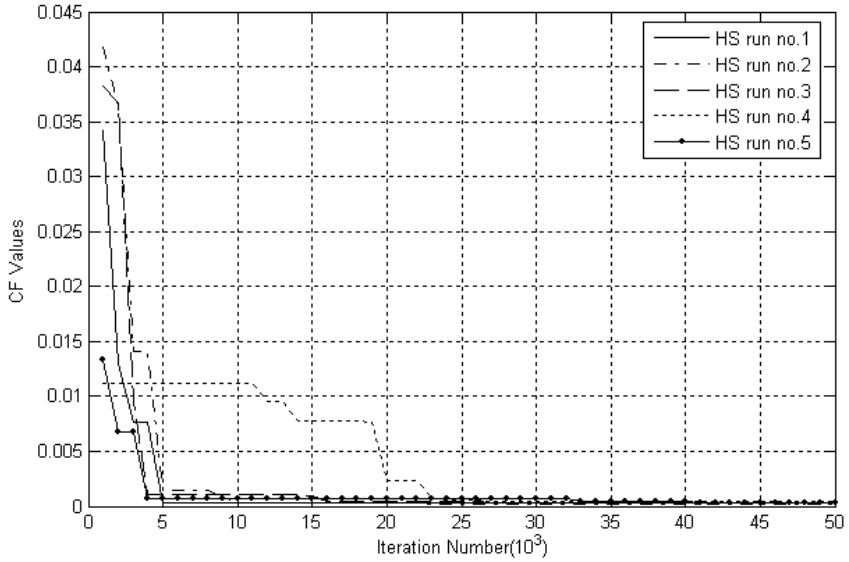

Figure 3.13 CF versus iteration number for HS algorithm (E96)

Table 3.6 Effects of DE own parameters on SVF design performance (E96)

CF Values (DE-E96)	*NP = 8*			***NP = 12***		
	CR = 0.3	*CR = 0.5*	*CR = 1*	*CR = 0.3*	***CR = 0.5***	*CR = 1*
F = 0.5	4.21 x10^{-5}	6.03 x10^{-4}	0.1092	2.55 x10^{-5}	**1.95 x10^{-5}**	0.0028
F = 1.0	7.79 x10^{-5}	6.15 x10^{-4}	0.0725	7.63x10^{-5}	3.12 x10^{-5}	0.064
F = 1.5	5.32 x10^{-5}	9.03 x10^{-5}	0.1537	1.6 x10^{-4}	7.25 x10^{-4}	0.0127
F = 2.0	9.01 x10^{-4}	3.7 x10^{-4}	0.048	9.12 x10^{-5}	1.78 x10^{-4}	0.00296

Table 3.7 Effects of HS own parameters on SVF design performance (E96)

CF Values (HS-E96)	***HMS = 5***			*HMS = 10*		
	HMCR = 0.3	*HMCR = 0.6*	***HMCR = 0.9***	*HMCR = 0.3*	*HMCR = 0.6*	*HMCR = 0.9*
PAR = 0.4- 0.9	2.3 x 10^{-4}	7.13 x 10^{-5}	**1.661 x 10^{-5}**	0.0025	0.0076	2.92 x 10^{-5}
PAR = 0.1- 0.9	7.2 x 10^{-4}	6.276 x 10^{-5}	9.97 x 10^{-5}	1.5 x 10^{-4}	0.002	2.414 x 10^{-5}
PAR = 0.1- 0.6	9.33 x 10^{-4}	5.2 x 10^{-4}	3.18 x 10^{-5}	4.6 x 10^{-4}	0.0013	5.01 x 10^{-5}

Exact values of discrete components, total error and computation time of DE and HS based design and previously used methods are tabulated in Table 3.8.

Following, we employed Monte Carlo and worst case analysis in order to investigate robustness of DE and HS based SVF design in case of component value variations due to specified tolerances of manufactured series. One hundred different trials of Monte Carlo simulations were applied by adding tolerance value of relevant manufacturing series for each analog filter structure where AC simulation results for ten trials are depicted in Figure 3.14, Figure 3.15, Figure 3.16 and Figure 3.17. Tolerance values are randomly chosen from %0 up to %5 which is the maximum value for E24 series. For E96 series; tolerance values are randomly chosen from %0 up to %1 which is the maximum value.

Table 3.8 Component values and performance of previous methods vs DE and HS algorithms for SVF design

	GA-E24 [30]	**PSO-E24 [30,31]**	**ABC-E24 [30]**	**DE-E24**	**HS-E24**	**GA-E96 [30]**	**PSO-E96 [30,31]**	**ABC-E96 [30]**	**DE-E96**	**HS-E96**
R1(kΩ)	43	10	62	560	43	69	10.2	59	953	95.3
R2(kΩ)	5.6	1.65	1	1.6	8.2	2.55	8.66	88.7	4.64	6.34
R3(kΩ)	24	30.11	91	30	33	65.3	14.7	54.9	7.87	4.42
R4(kΩ)	280	212	4.3	750	7.5	237	187	90.9	442	57.6
R5(kΩ)	4.4	1.039	27	4.7	27	2.87	1.13	10	4.22	97.6
R6(kΩ)	9.2	3.9	1.8	62	13	1.43	2.94	51.1	2.94	42.2
C1(nF)	180	470	2.7	390	2.7	110	464	7.5	953	9.53
C2(nF)	16	37	3.6	2.2	2.4	80.4	82.5	4.32	47.5	3.32
Total Error (x10^{-4})	2.2	3.6	3.8	**0.32**	1.9	1.1	3.1	0.17	0.19	**0.16**
Computation Time	5.2 min	4.5 min	3.4 s	36.7 s	79.8 s	7.4 min	5.6 min	2.6 s	50 s	102.7 s

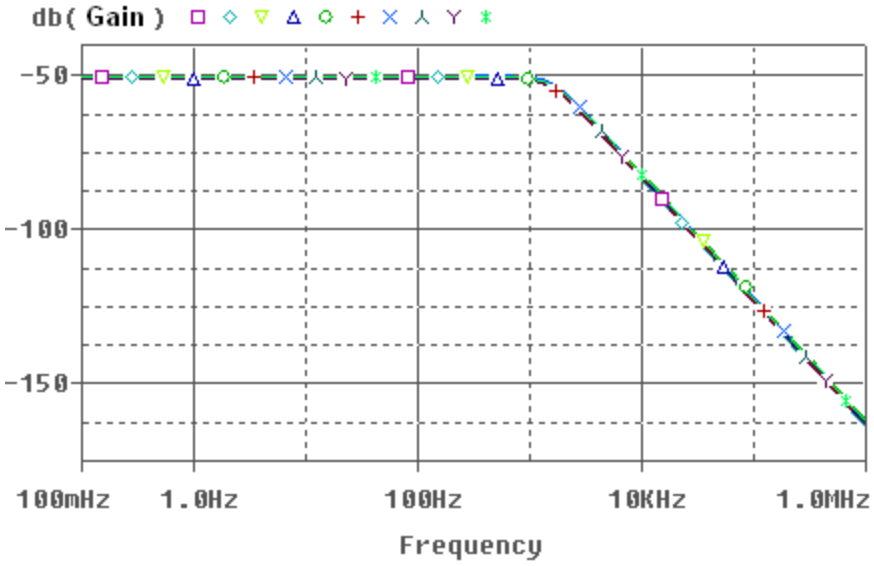

Figure 3.14 Monte Carlo analysis for DE based SVF design (E24)

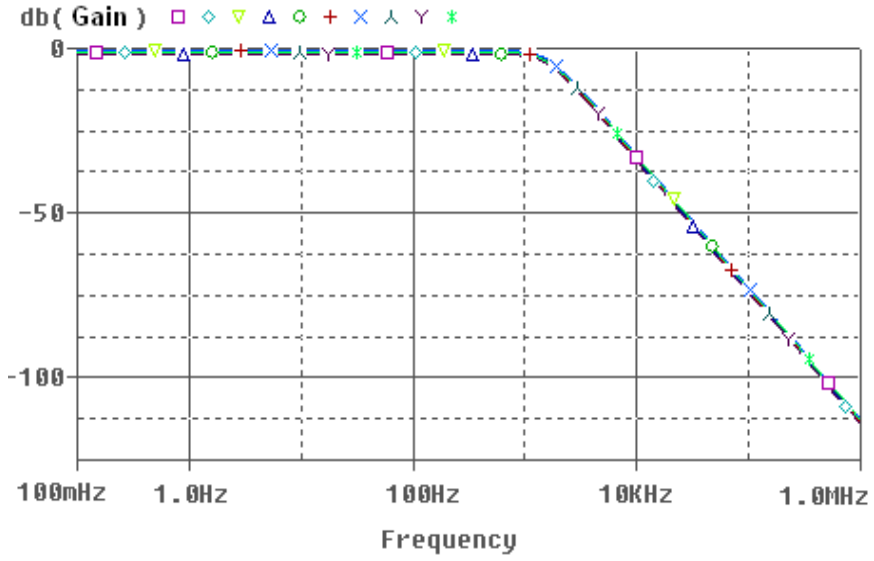

Figure 3.15 Monte Carlo analysis for HS based SVF design (E24)

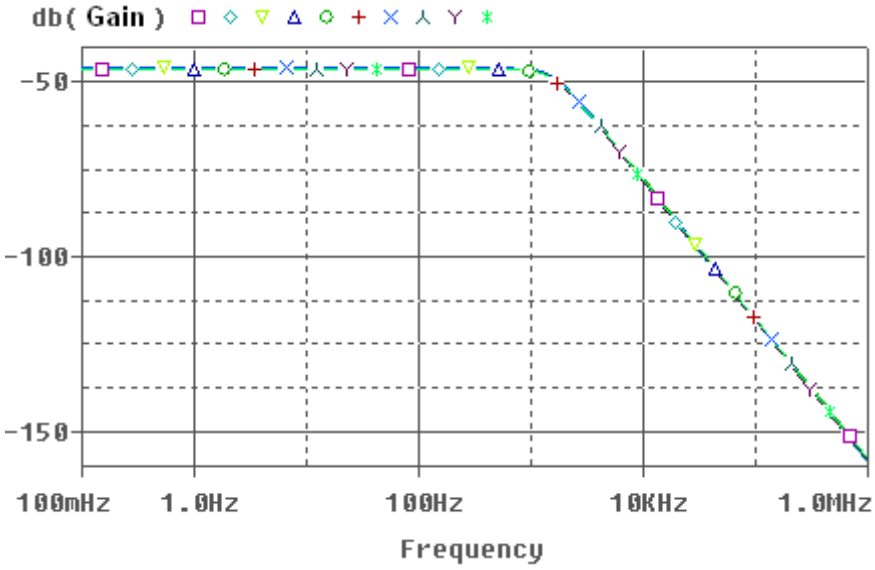

Figure 3.16 Monte Carlo analysis for DE based SVF design (E96)

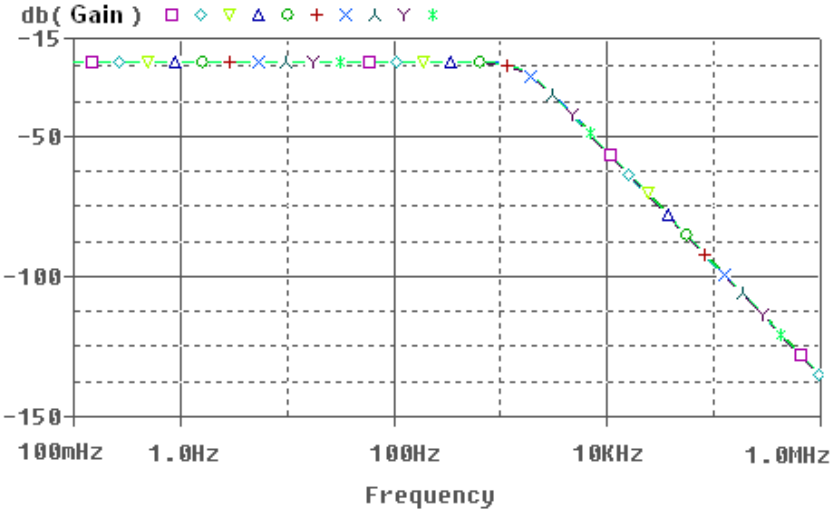

Figure 3.17 Monte Carlo analysis for HS based SVF design (E96)

For the last step we tabulated worst case analysis for Butterworth filter and SVF. Worst case analysis is one of the most important elements needed to ensure reliable operation of electronic circuits and systems. In this study, it is used to determine the worst possible cut-off frequency values in case of the greatest component tolerance arising from manufacturing series. The worst case errors of cut-off frequency variations for nature inspired metaheuristics based analog filter design are calculated using (3.18) and tabulated in Table 3.9.

$$Error_{WorstCase(f_0)} = \left| \frac{f_{0(actual)} - f_{0(WorstCase)}}{f_{0(actual)}} \right| \quad (3.18)$$

From Table 3.9, it can be seen that the greatest worst case error arises in Butterworth design case. SVF filter design schemes are more robust with respect to previous case. However it has to be noted that E12 series utilized in Butterworth design involves a greater tolerance value than E24 and E96 series utilized in SVF design. Therefore, it is obvious that worst case design error decreases as component tolerance value decreases. Maximum tolerance values (%10 for E12, %5 for E24, %1 for E96) are used for the worst case scenario.

Table 3.9 Worst case cutoff frequency values of DE and HS based design

	HS	**DE**
Butterworth Filter (E12)	0.193	0.193
SVF (E24)	0.045	0.077
SVF (E96)	0.037	0.037

3.3 Summary

Automation of analog active filter optimization is a very challenging and a time consuming task. The emphasis of this work is creating designs using actually existing components, which will yield feasible circuits. The performances of two nature-inspired metaheuristics on analog filter design have been explored comprehensively. DE and HS algorithms were utilized for both 4th order Butterworth low pass filter and 2nd order SVF design and were investigated for the selection of passive components from different manufactured series by means of accuracy and execution time. Considering Butterworth filter design, both algorithms minimized the total design error with respect to previous methods. Components of SVF are selected from both E24 and E96 series in order to investigate whether performance of DE and HS will be affected when same topology is designed with different series. Considering SVF design with E24

series, DE successfully minimized the design error in a short computation time. Box and whisker plots also demonstrate that variation of CF values obtained with DE method is the smallest when multiple runs are of concern. HS obtained the minimum design error when components are selected from E96 series. In addition, the optimal parameter set of both algorithms with exception of C_R of DE remains unchanged for SVF design with different manufactured series. Monte Carlo and worst case analysis results are also presented in order to demonstrate the robustness of the proposed approaches especially for SVF design.

Future directions would be to evaluate the optimization performance of metaheuristics on more complex analog circuit structures with particular design constraints and specifications

CHAPTER 4

EVOLUTIONARY ALGORITHMS FOR ANALOG INTEGRATED CIRCUIT DESIGN

Analog IC design is a challenging process which involves the characterization of complex tradeoffs between nonlinear objectives and also satisfying required constraints. Those objectives are comprised of design parameters which are ideally accepted as variables and optimum solution set is searched. However, as the circuit complexity increases the search space expands such that obtaining the optimal combination of design parameters by hand becomes a time consuming and unaffordable process. Considering CMOS IC design process, there are several relations that should hold between length, width and width/length ratios of MOS transistors to ensure that the search space is smooth and the optimization process is reliable. Therefore, efficient optimization methods are required for automation of optimal sizing of CMOS analog IC design [52].

In this study, we will use HS and DE as optimization method for automation of optimal sizing of differential amplifier, operational amplifier and comparator circuits. Simulations are performed with TSMC 0.35 μm technology parameters in MATLAB environment with Intel Core 2 Duo CPU, T7300 @ 2.00GHz.

4.1 EA Based CMOS Differential Amplifier Design

4.1.1 Differential Amplifier Structure

The problem considered here is the optimal selection of transistor dimensions, which is only a part of a complete analog circuit CAD tool. Actually, analog sizing is a constructive procedure that aims at mapping the circuit specifications (objectives and

constraints on performances) into the design parameter values [53]. In other words, the performance metrics of the circuit, such as gain, power dissipation, occupied area, etc. have to be formulated in terms of the design parameters [54]. Then, these design parameters such as device sizes and bias currents should be adjusted under multiple design objectives and constraints. The many degrees of freedom in parameter space as well as the need for repeated circuit performance evaluation made this a lengthy and tedious process [55]. Here, particular specifications for specified topology of a differential amplifier is aimed to be met by adjusting design parameters such as device sizes and bias currents with HS and DE algorithms, while minimizing the total MOS transistor area.

The configuration considered here is a differential amplifier with a current mirror load (Figure 4.1) and this circuit can be characterized by a number of specifications as given below. More detailed description can be found in [56], [57], [2] and [58].

- Common Mode Rejection Ratio (CMRR)
- Input Offset Voltage (V_{OS})
- Slew Rate (SR)
- Power Dissipation (P_{diss})
- Small Signal Characteristics (A_v , ω_{-3dB} , f_t , f_{-3dB})
- Input Common Mode Range (ICMR)
- Power Supply Rejection Ratio(PSRR)

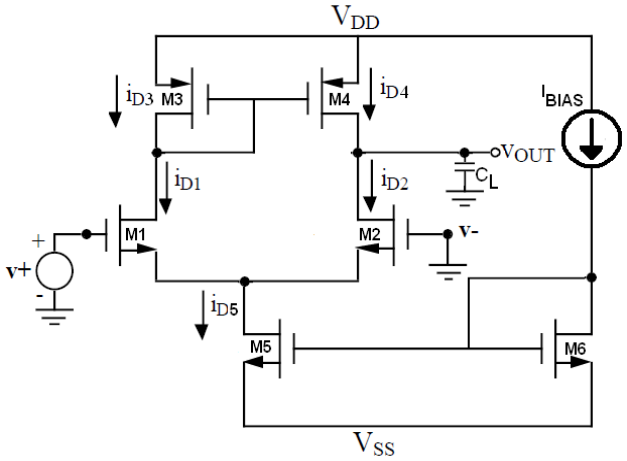

Figure 4.1 Differential amplifier with current mirror load [58]

Small-signal differential voltage gain (A_v), cut-off frequency (f_{-3dB}), unity gain bandwidth (f_t), maximum and minimum input common mode range voltages ($V_{IC(max)}$, $V_{IC(min)}$), slew rate (SR) and power dissipation (P_{diss}) as design specifications and output capacitance (C_L), compensation capacitance (C_c) and MOS transistor dimensions as design parameters are provided within limits. Equations defining each specification [57], [2], [58] are utilized for cost function (4.1) of HS and DE based analog IC design and are considered for obtaining MOS device sizes and moreover minimizing the total MOS transistor area. i in (4.1) indicates the number of each transistor (i = 1..6). T is the total number of transistors which is 6 for differential amplifier in Figure 4.1.

$$CF = \sum_{i=1}^{T} \left(W_{(i)} x L_{(i)} \right) \tag{4.1}$$

Following is constraints and objectives for differential amplifier.

- Determination the range of I_{d5} (I_{ss}) to satisfy both SR and P_{diss}.
- Design of W1/L1 (W2/L2) to satisfy A_v
- Design of W3/L3 (W4/L4) to satisfy the upper ICMR
- Design of W5/L5 (W6/L6) to satisfy the lower ICMR

4.1.2 Simulation Results

DE and HS are utilized for a differential amplifier with current mirror load having design specifications of SR≥10V/μs (C_L=10pF), f_{-3dB}≥100kHz (C_L=5pF), -1.5V≤$ICMR$≤2V, A_v>100 V/V, P_{diss}≤2.5mW with inputs V_{DD}=-V_{SS}=2.5V, V_{tn}=0.4761V, V_{tp}=-0.6513V, K'_n=181.2μA/V^2, K'_p= 65.8μA/V^2, λ_n=0.04 V^{-1}, λ_p=0.05 V^{-1}. Constraints for design variables are set as C_L>=10 pF, 100≥(W/L)$_i$≥2 (i=1..6), L_i=*1.4 μm*.

Considering both DE and HS particle vector structure is expressed in (4.2).

$$x = [SR, C_L, A_v, f_{-3dB}, V_{icmin}, V_{icmax} P_{diss}] \tag{4.2}$$

Target value of CF is aimed to be smaller than 300 μm^2. DE based design method resulted in a total MOS transistor area of 185 μm^2 along with exact values of design specification and design variables (W_i, I_{bias}, C_L) as tabulated in Table 4.1. Despite the

fact that DE resulted in shortest computation time minimum MOS transistor area is obtained with HS method when compared with DE and previous works. Algorithm parameters and computational performance for metaheuristics are tabulated in Table 4.2. Simulation results show that both DE and HS resulted in shorter computational time than PSO. ICMR and cut-off frequency values of DE based design method are also improved when compared to that of PSO as given in Table 4.3. Figures 4.2- 4.11 demonstrate that SPICE Simulator validates the EA based design results as design specifications are met.

Table 4.1 Design variable obtained with metaheuristics

Design Variables	**Darwin [59]**	**PSO [52]**	**HS**	**DE**
I_{bias} *(µA)*	2	125	88	153.5
W_1/L_1, W_2/L_2 *(µm/µm)*	240/13.2	29.4/3.5	17.5/1.4	51.1/1.4
W_3/L_3, W_4/L_4 *(µm/µm)*	7.3/7.7	11.3/3.5	2.8/1.4	10.1/1.4
W_5/L_5 *(µm/µm)*	4.6/2.4	4.2/1.4	2.8/1.4	4.9/1.4
W_6/L_6 *(µm/µm)*	4.6/2.4	4.2/1.4	2.8/1.4	4.9/1.4
C_L *(pF)*	2	5	5	7

Table 4.2 Comparison of computational performance

	PSO [52]	**DE**	**HS**
Computation Time	25.02 s	0.047 s	0.25 s
Iterations	582	7	1000
Parameters	NP: 10	NP : 10	HMS: 6
	c_1:1.7, c_2:1.7	CR : 1.0	HCMR: 0.9
	w(inertia)=0.9	F : 0.85	PAR: 0.4-0.9

Table 4.3 Comparison of previous methods with DE and HS by means of design criteria

Design Criteria	Specs	DARWIN [59]	PSO [52] (SPICE)	HS (SPICE)	DE (SPICE)
Output Capacitance (pF)	≥5	2	5	5.0107	6.9855
Slew Rate (V/µs)	≥ 10	3.2	22.4	14.916	21.248
Power Dissipation (µW)	≤ 2000	31	1260	886	1540
Phase Margin (^{o})	> 45	72	83.8	89.1	87.33
Cut-off Frequency (KHz)	≥100	-	100	114	162
Gain (dB)	> 40	60	42	40.98	42.175
Vic_{min} (V)	≥-1.5	-1.3	-0.8	-0.7	-0.8
Vic_{max} (V)	≤2	1.9	1.4	1.2	1.63
CMRR (dB)	> 40	-	84.2	78.5	83.9603
$PSRR^+$ (dB)	>40	-	40.1	42.93	44.05
$PSRR^-$ (dB)	>40	-	68	67.64	67.04
MOS Area ($x10^{-10}$ m^2)	**<3**	**65**	**2.96**	**0.65**	**1.85**

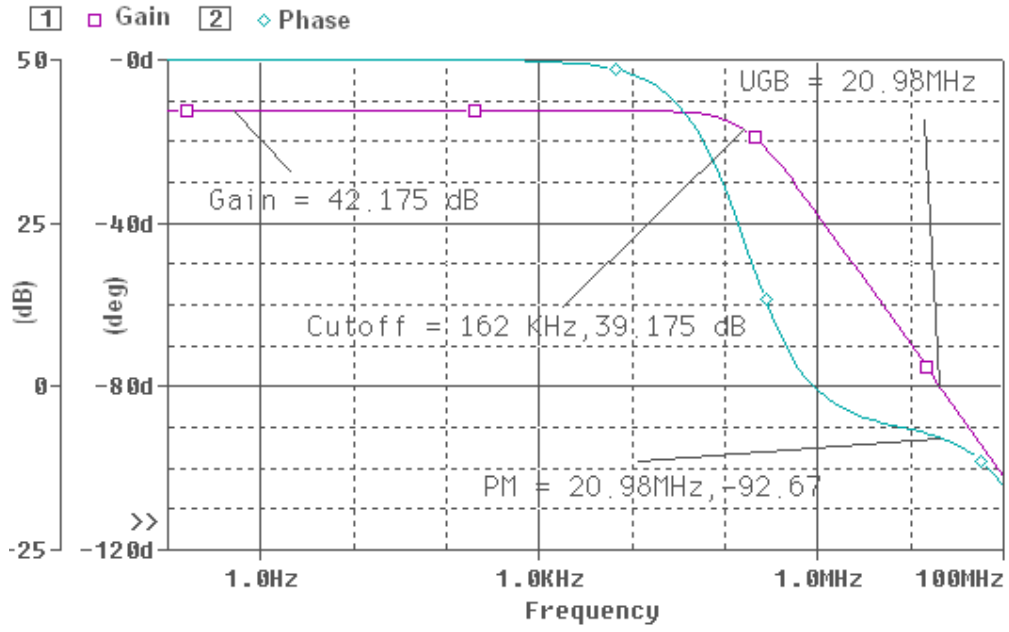

Figure 4.2 Gain and phase margin of DE based differential amplifier

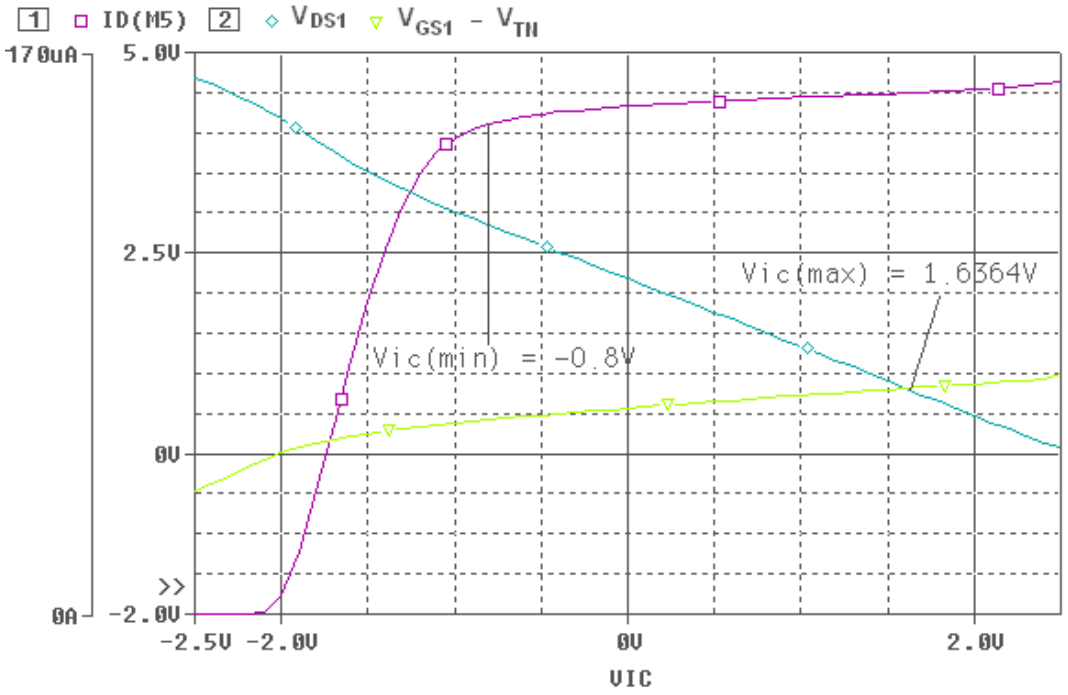

Figure 4.3 ICMR of DE based differential amplifier

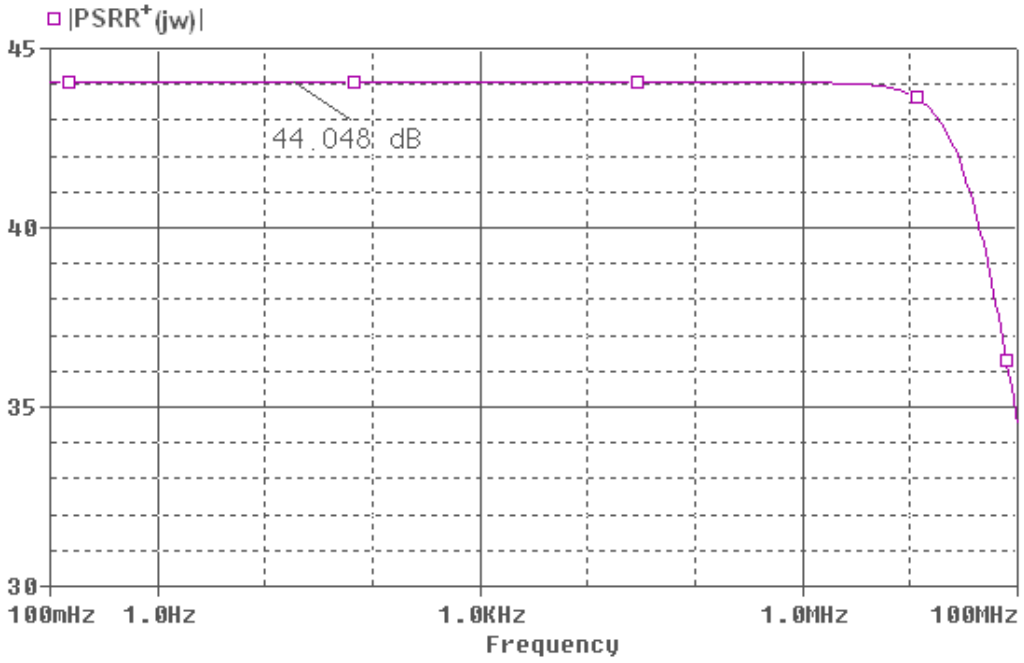

Figure 4.4 PSRR^{+} of DE based differential amplifier

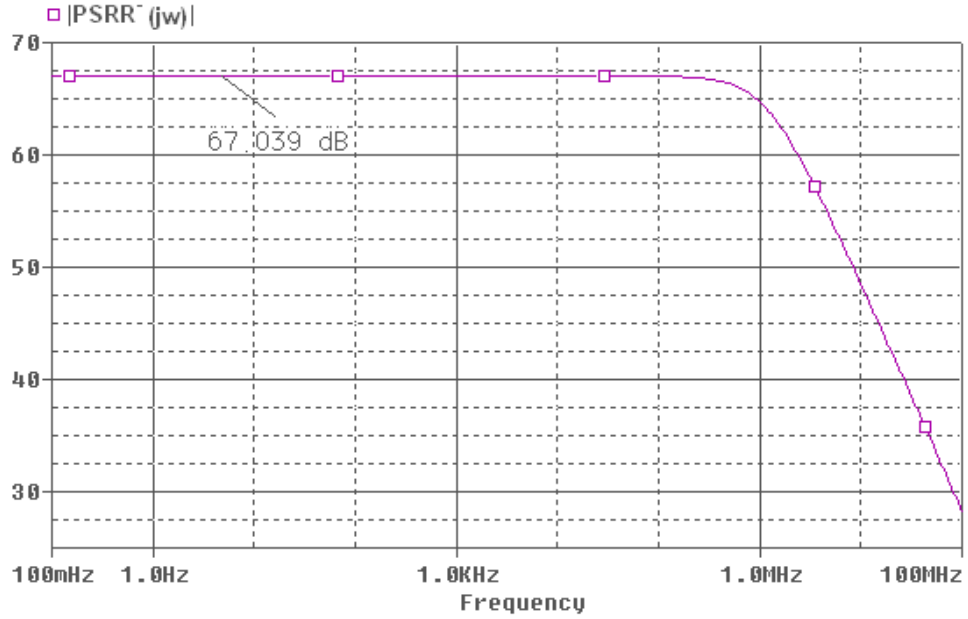

Figure 4.5 PSRR⁻ of DE based differential amplifier

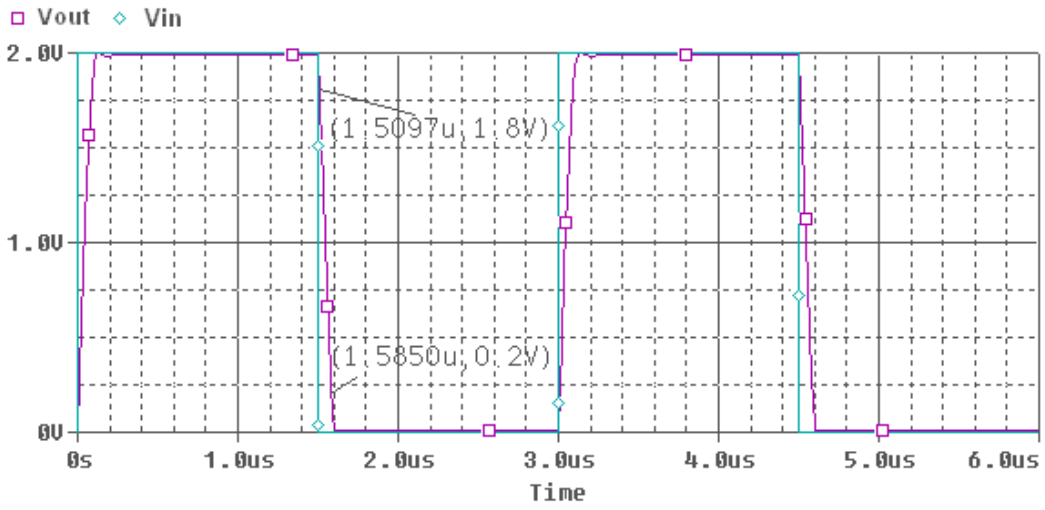

Figure 4.6 Slew rate of DE based two-stage differential amplifier

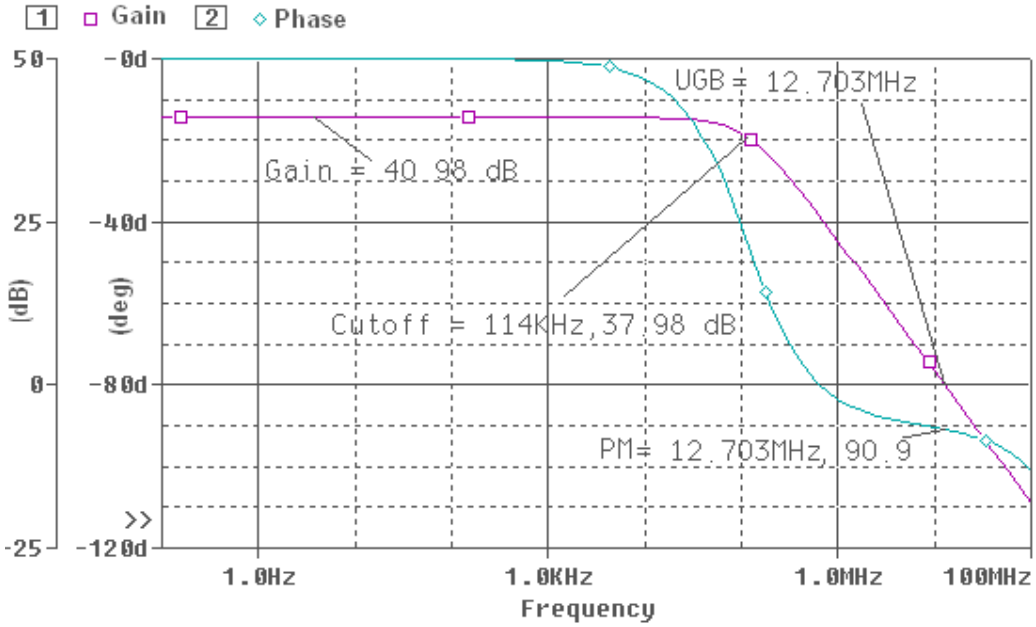

Figure 4.7 Gain and phase margin of HS based differential amplifier

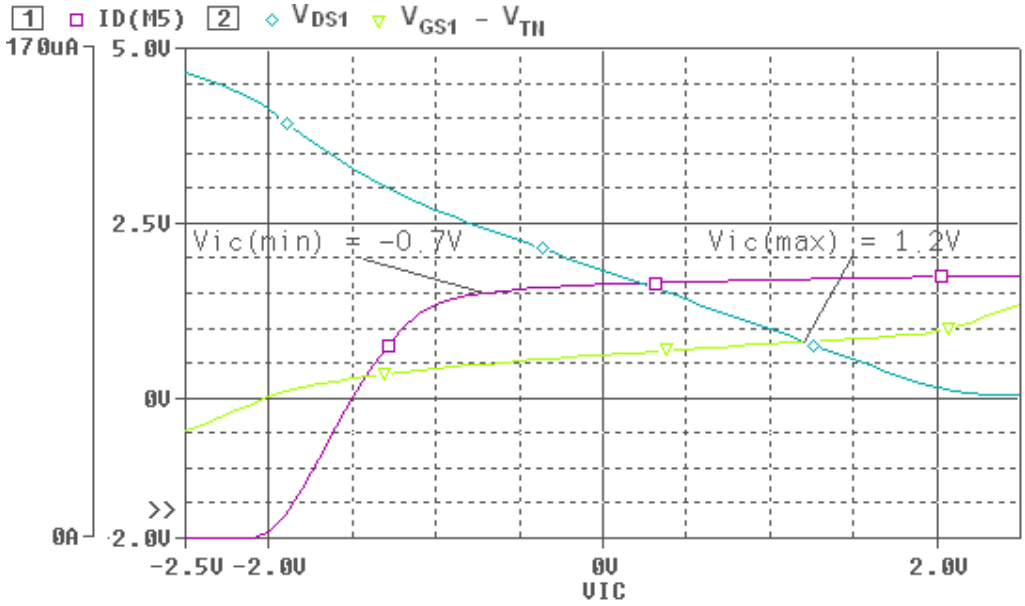

Figure 4.8 ICMR of HS based differential amplifier

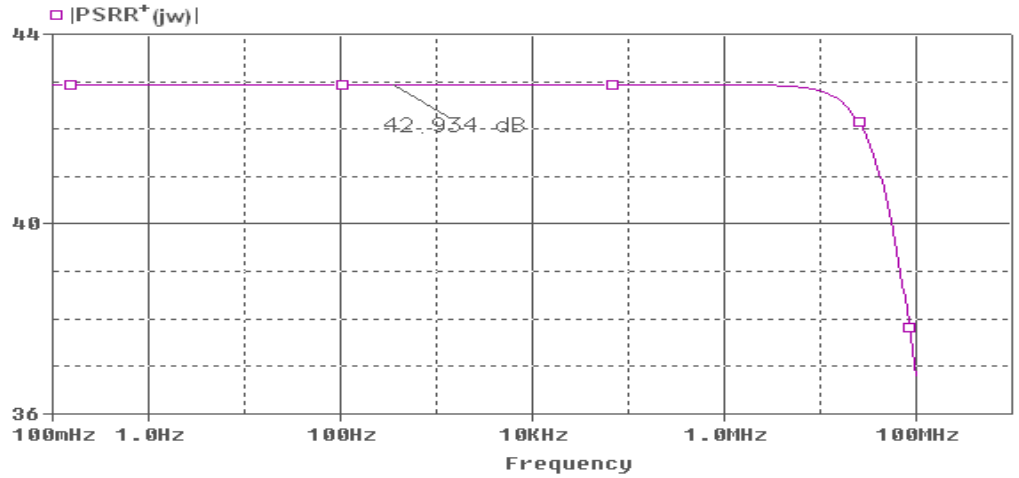

Figure 4.9 PSRR^{+} of HS based differential amplifier

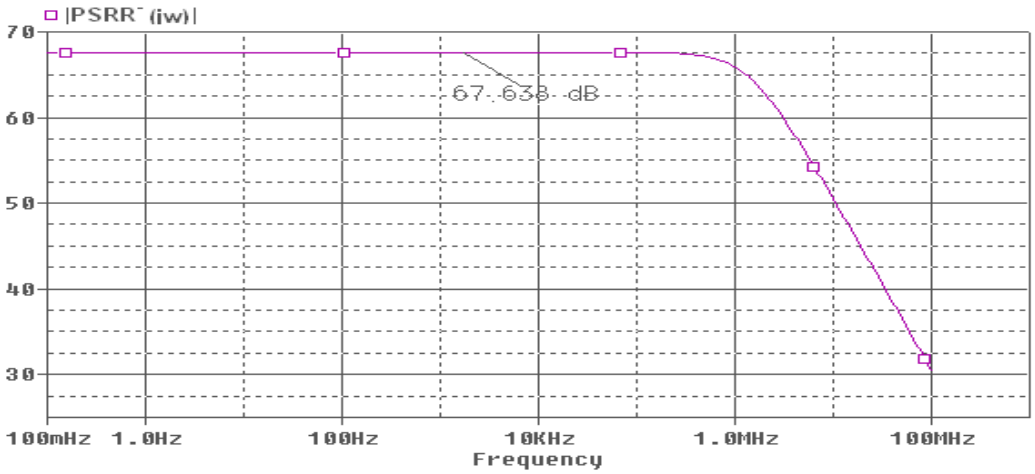

Figure 4.10 PSRR^{-} of HS based differential amplifier

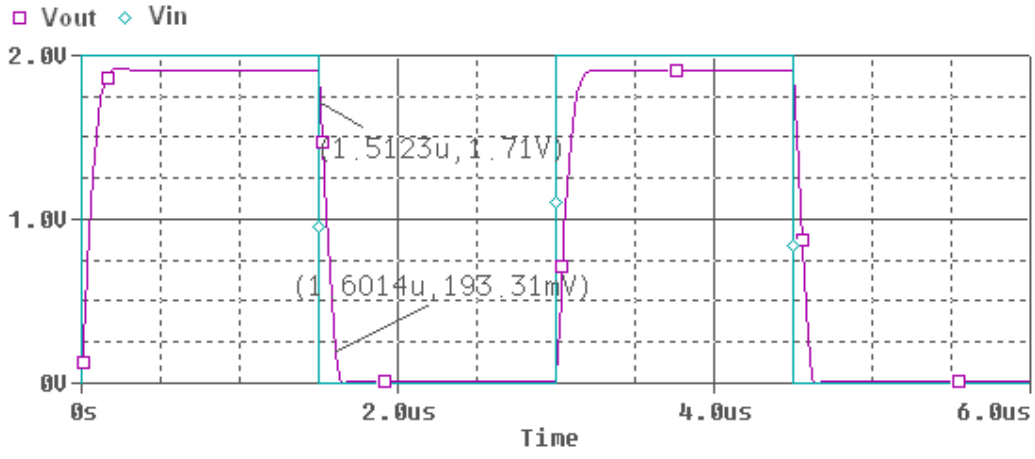

Figure 4.11 Slew rate of HS based two-stage differential amplifier

4.2 EA Based CMOS Operational Amplifier Design

4.2.1 Operational Amplifier Structure

The configuration considered in this part is a two stage CMOS operational amplifier (op-amp) (Figure 4.12). This circuit can be characterized by a number of specifications as given below. More detailed description can be found in [56], [57], [2] and [58].

- Common Mode Rejection Ratio (CMRR)
- Input Offset Voltage (V_{OS})
- Slew Rate (SR)
- Power Dissipation (P_{diss})
- Small Signal Characteristics (Av , ω_{-3dB} , ft , f_{-3dB})
- Input Common Mode Range (ICMR)
- Power Supply Rejection Ratio(PSRR)

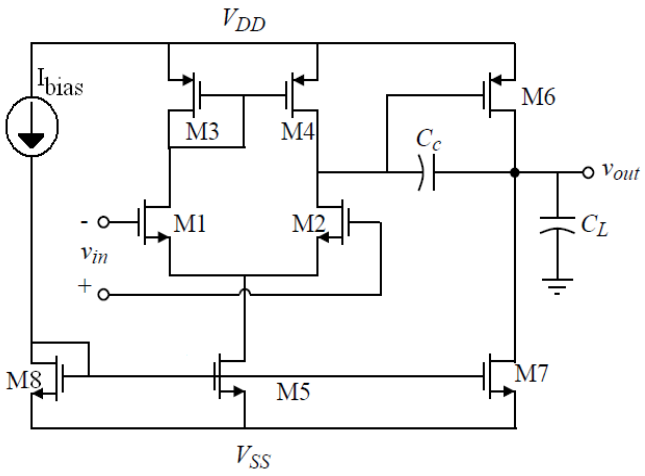

Figure 4.12 Two stage operational amplifier [58]

Following is constraints and objectives for operational amplifier.

- Selection of minimum value for *Cc*.
- Determination of I_{d5} (I_{ss}) to satisfy *SR*
- Design of W1/L1 (W2/L2) using the transconductance of the differential input stage
- Design of W3/L3 (W4/L4) to satisfy the upper ICMR

- Design of W5/L5 (W8/L8) to satisfy the lower ICMR
- Design of W6/L6 assuming balanced conditions

$$(W_6 / L_6) = (W_4 / L_4)\frac{g_{m6}}{g_{m4}} \tag{4.3}$$

where

$$g_{m6} \geq 10 g_{m1} \tag{4.4}$$

and

$$g_{m1} = 2\pi f_t C_c \tag{4.5}$$

assuming zero z_1 is placed beyond ten times f_t [58]

$$g_{m4} = \sqrt{2K_4^{'}(W_4 / L_4) I_{d4}} \tag{4.6}$$

- Calculation of I_{d6} which will most likely determine the majority of the power dissipation.

$$I_{d6} = \frac{g_{m6}^2}{2K_6^{'}(W_6 / L_6)} \tag{4.7}$$

- Design of W7/L7 to achieve the desired current ratios between I_{d5} and I_{d6}

$$(W_7 / L_7) = (W_5 / L_5)\frac{I_6}{I_5} \tag{4.8}$$

4.2.2 Simulation Results

Considering two stage operational amplifier, only DE is utilized for design specifications of SR≥10V/µs, f_t≥3MHz, A_v>1000 V/V, -1.5V≤ ICMR≤2V, P_{diss}≤2.5mW with the inputs and particle vector structure as same with previous design scheme. Constraints for design parameters are set as C_L>=10 pF, $100 \geq (W/L)_k \geq 2$ (k=1..8). In order to minimize the channel modulation effect, all MOSFET length values are chosen as *2 µm* [60]. Since there is another study going on simultaneously for designing operational amplifier with HS algorithm, we didn't consider HS for our study.

Target value of CF is aimed to be smaller than 300 µm^2. DE based design method resulted in a total MOS transistor area of 259 µm^2 which is minimum area compared with PSO, along with exact values of design specification and design variables (W_k, I_{bias}, C_L) as tabulated in Table 4.4. DE resulted in shorter computation time than PSO as

tabulated in Table 4.5. Comparison of previous methods with DE by means of design criteria is given in Table 4.6. Figures 4.13- 4.17 demonstrate that SPICE Simulator validates the DE based design results as design specifications are met.

Table 4.4 Design variable obtained with metaheuristics

Two-Stage Op-amp Design Parameters	**Convex opt. [59]**	**PSO [52]**	**DE**
I_{bias} *(µA)*	10	40.39	39.1506
W1/L1, W2/L2 (µm/µm)	232.8/0.8	4.9/2	3.2056/2
W3/L3, W4/L4 (µm/µm)	143.6/0.8	5.9/2	6.9662/2
W5/L5 (µm/µm)	64.6/0.8	2.1/2	3.1130/2
W6/L6 (µm/µm)	588.8/0.8	90.9/2	84.1094/2
W7/L7 (µm/µm)	132.6/0.8	16.3/2	18.7930/2
W8/L8 (µm/µm)	2/0.8	2.1/2	3.1130/2
C_L *(pF)*	3	10	10
C_c *(pF)*	3.5	3	3

Table 4.5 Comparison of computational performance

	PSO [52]	**DE**
Time	8.6 s	4.594 s
Iterations	100	677
Parameters	NP: 10	NP : 10
	c_1:1.7, c_2:1.7	CR : 1.0
	w(inertia)=0.9	F : 0.85

Table 4.6 Comparison of previous works with DE by means of design criteria

Two-stage OPAMP Design Criteria	**Specs**	**Convex Opt. [59]**	**PSO [52] (SPICE)**	**DE (SPICE)**
Output Capacitance (pF)	≥10	3	10	10
Slew Rate (V/µs)	≥ 10	88	11.13	10.53
Power Dissipation (µW)	≤ 2500	5000	2370	1860
Phase Magrin (^{o})	>45	60	66.55	69.092
Unity Gain BW (MHz)	≥3	86	5.32	4.1011
Gain (dB)	> 60	89.2	63.8	60.393
Vic_{min} (V)	≥-1.5	-	-0.8	-0.813
Vic_{max} (V)	≤2	-	1.75	1.8155
CMRR (dB)	> 60	92.5	83.74	81.4793
$PSRR^{+}$ (dB)	>70	116	78.27	75.605
$PSRR^{-}$ (dB)	>70	98.4	93.56	93.782
Output Resistance (kΩ)	>200	-	751	790.8
Total Area ($x10^{-10}$ m^2)	**< 3**	**82**	**2.65**	**2.59**

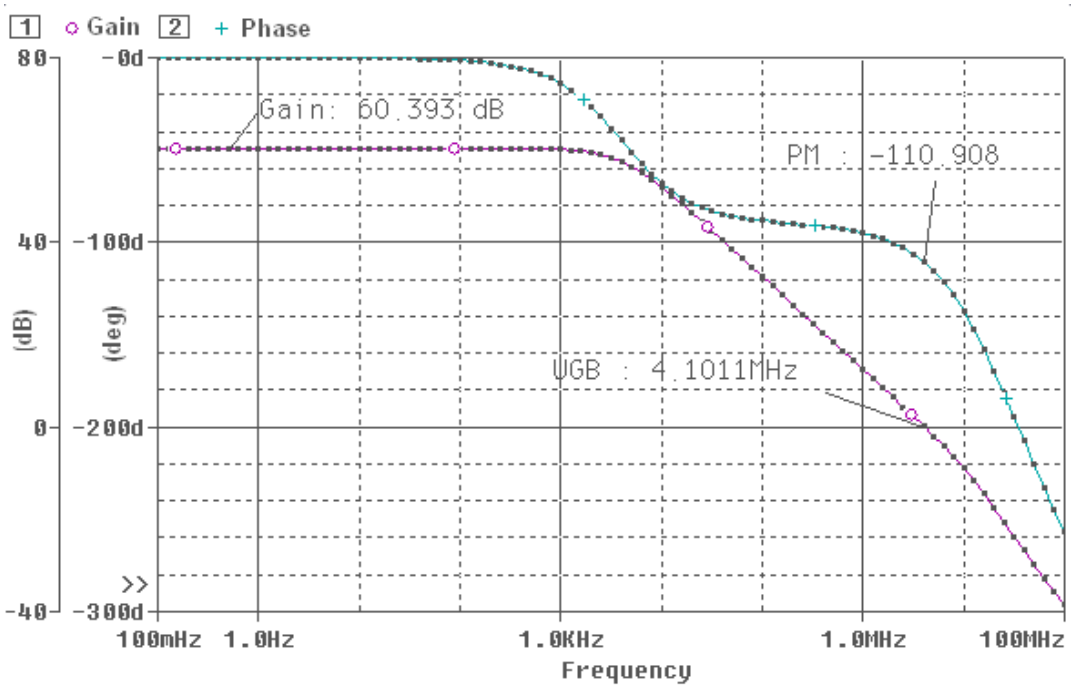

Figure 4.13 Gain and phase margin of DE based operational amplifier

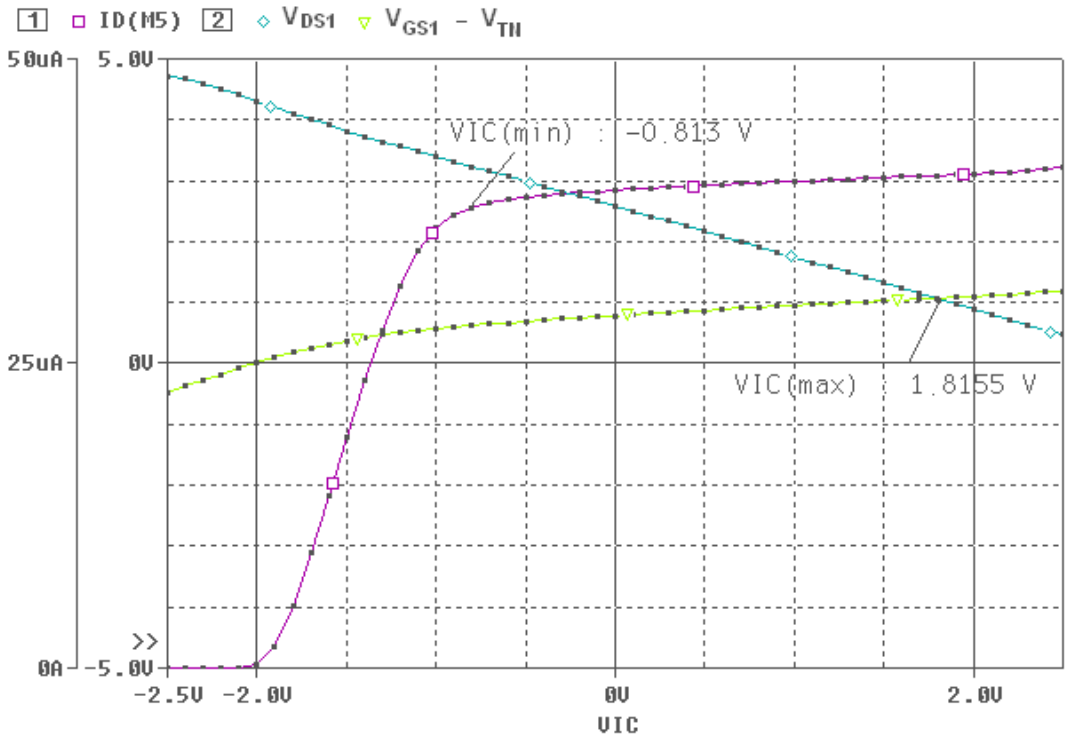

Figure 4.14 ICMR of DE based operational amplifier

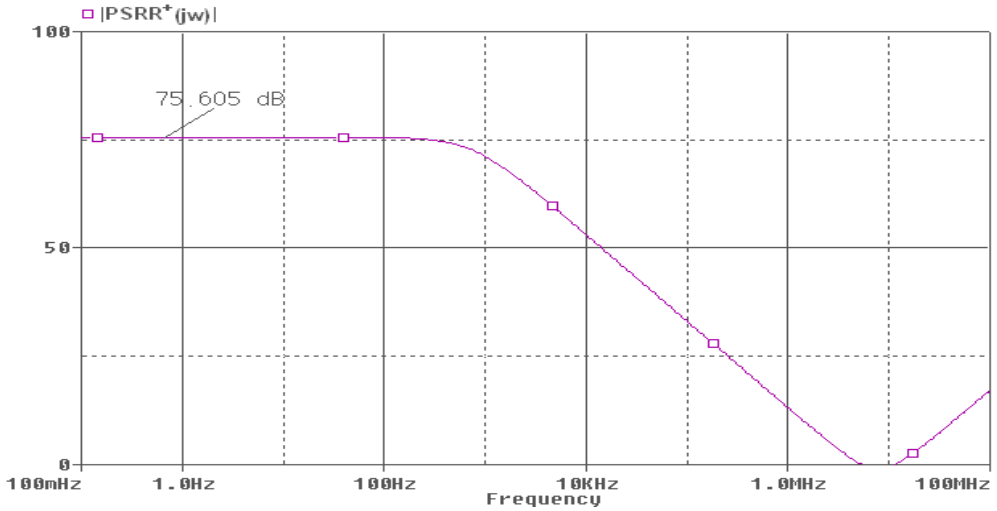

Figure 4.15 PSRR^{+} of DE based operational amplifier

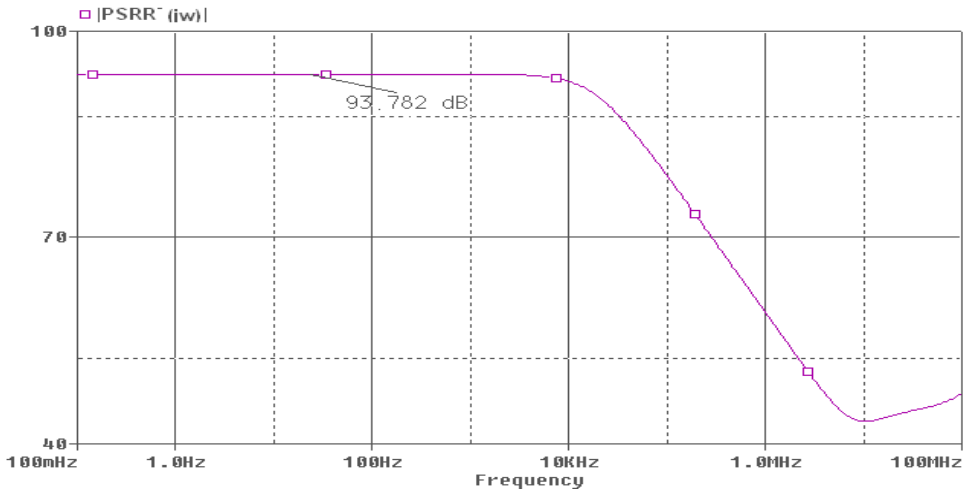

Figure 4.16 PSRR^{-} of DE based operational amplifier

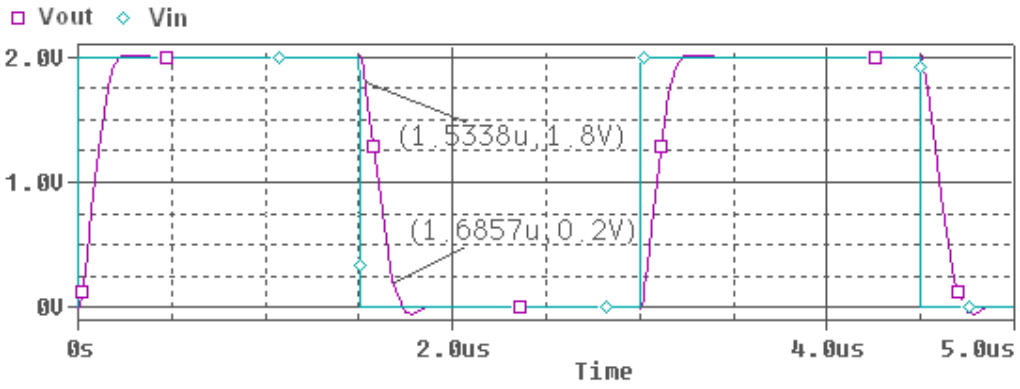

Figure 4.17 Slew rate of DE based two-stage operational amplifier

4.3 EA Based CMOS Comparator Design

As a last step of this study, a comparator is designed with HS and DE algorithms. The configuration considered here is comparator with PMOS input driver (Figure 4.18) where details can be found in [61].

4.3.1 CMOS Comparator Structure

A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. They are commonly used in devices such as Analog-to-digital converters (ADCs).

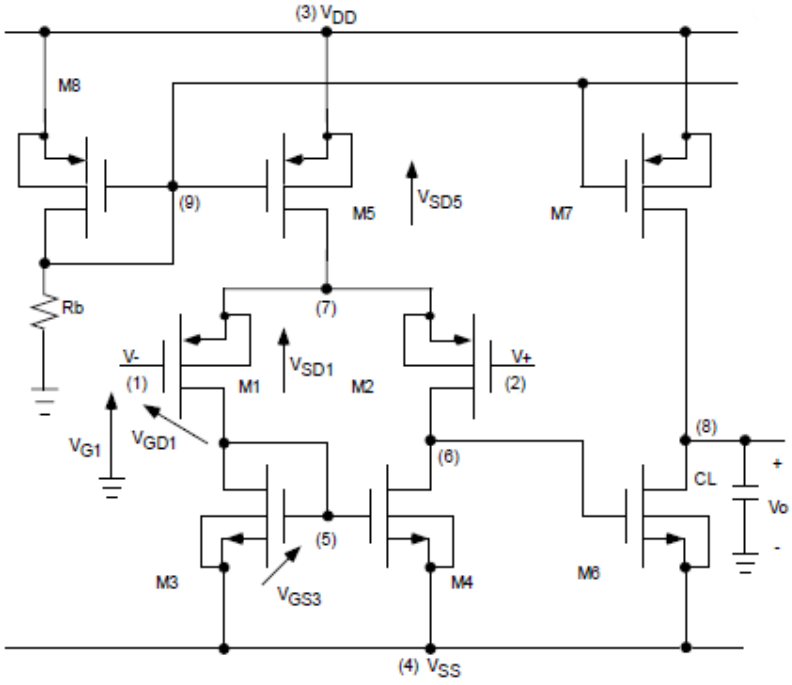

Figure 4.18 CMOS comparator with PMOS input driver

Design specifications are VDD=2.5V, VSS=-2.5V, AV>10000, -1.75<CMR<1.75, -2.25<Vo<2.25, SR>10V/us. Following is constraints and objectives for comparator.

- Determine the current drive requirement of $(W/L)_7$ to satisfy the SR specification.

$$I_{D7} = C_L\left(\frac{dV}{dt}\right) = C_L(SR) \tag{4.9}$$

- Determine the size of $(W/L)_6$ and $(W/L)_7$ to satisfy the output-voltage swing requirement.

$$(W/L)_7 = \frac{2I_{DS7}}{K_P\left(V_{DS7(SAT)}\right)^2} \tag{4.10}$$

$$(W/L)_6 = \frac{2I_{DS6}}{K_P\left(V_{DS6(SAT)}\right)^2} \tag{4.11}$$

- Calculate the gain of the second stage.

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right) \tag{4.12}$$

- Calculate the gain of the first stage to satisfy the overall gain.

$$A_V = A_{V1}A_{V2} \geq 10000 \tag{4.13}$$

- Determine the first stage biasing current using the minimum allowable size of 1, and minimum output offset. Consider $(W/L)_4$ and $(W/L)_6$; using the minimum size for $(W/L)_4$, determine the current I_{SD4} that mirror with $(W/L)_6$. That is,

$$I_{DS4} = \frac{(W/L)_4}{(W/L)_6} I_{DS6} \tag{4.14}$$

$$I_{SD5} = 2I_{DS4} \tag{4.15}$$

and consider $(W/L)_5$ and $(W/L)_7$; using the minimum size for $(W/L)_5$, determine the current I_{DS5} that mirror with $(W/L)_7$. That is,

$$I_{SD5} = \frac{(W/L)_5}{(W/L)_7} I_{SD7} \tag{4.16}$$

$$I_{DS4} = I_{SD5}/2 = I_{DS3} \tag{4.17}$$

$$I_{SD2} = I_{SD1} = I_{SD5}/2 \tag{4.18}$$

finally select the larger of the two I_{SD4} and adjust the size of $(W/L)_4$ if necessary.

- Determine the size of $(W/L)_1$ to satisfy the gain requirement.

$$(W/L)_1 = \frac{[A_{V1} I_{SD1} (\lambda_N + \lambda_P)]^2}{2K_P I_{SD1}} \tag{4.19}$$

- The minimum size of $(W/L)_5$ can be adjusted to satisfy the positive input CMR.

$$V_{SD5(SAT)} = V_{DD} - V_{G1(\max)} - \sqrt{\frac{2I_{SD1}}{K_P (W/L)_1}} - |V_{T1}| \tag{4.20}$$

$$(W/L)_5 = \frac{2I_{SD5}}{K_P (V_{DS5(SAT)})^2} \tag{4.21}$$

Select the larger of the two, $(W/L)_5$ and adjust the size of $(W/L)_7$ for proper mirroring with $(W/L)_5$.

$$(W/L)_7 = \frac{I_7}{I_5} (W/L)_5 \tag{4.22}$$

- The size of $(W/L)_3$ or $(W/L)_4$ can be adjusted to meet the negative input CMR.

$$(W/L)_3 = \frac{2I_{DS3}}{K_P (V_{G1(\min)} - V_{SS} - V_{T3} + |V_{T1}|)^2} \tag{4.23}$$

Select the larger of the two $(W/L)_3$.

- Determine the size of $(W/L)_8$ to provide as the main current mirror for the comparator.

$$(W/L)_8 = \frac{2I_{SD8}}{K_P (V_{SG8} - V_{TP})^2} \tag{4.24}$$

- The external resistor Rb connected between V_{G8} and ground must be chosen to provide the required current for $(W/L)_8$.

$$R_b = \frac{V_{G8} - 0}{I_{DS8}} \tag{4.25}$$

4.3.2 Simulation Results

Considering CMOS comparator, DE and HS are utilized for design specifications of VDD=2.5V, VSS=-2.5V, AV>10000, -1.75<CMR<1.75, -2.25<Vo<2.25, SR>10V/us. In order to minimize the channel modulation effect, all MOSFET length values are chosen as *2 µm* [60]. Target value of CF is aimed to be smaller than 500 μm^2. HS based design method resulted in a total MOS transistor area of 457 μm^2 which is minimum area compared with DE, along with exact values of design specification and design variables as tabulated below.

Table 4.7 Comparison of computational performance

	DE	**HS**
Time	0.469 s	4.641 s
Iterations	21	2000
Parameters	NP : 10	HMS: 6
	CR : 1.0	HMCR: 0.9
	F : 0.85	PAR: 0.4-0.9

Table 4.8 Design variables obtained with metaheuristics

COMPARATOR Design Parameters	**DE**	**HS**
W1/L1, W2/L2 (µm/µm)	20.057/2	24.230/2
W3/L3, W4/L4 (µm/µm)	2/2	2/2
W5/L5 (µm/µm)	6.899/2	6.386/2
W6/L6 (µm/µm)	58.396/2	58182/2
W7/L7 (µm/µm)	100.72/2	92.894/2
W8/L8 (µm/µm)	20.071/2	18.579/2
C_L *(pF)*	10.04	10
Rb (kΩ)	68.383	67.827

DE resulted in shorter computation time than HS as tabulated in Table 4.7. Performance of DE and HS algorithms and design variables obtained with metaheuristics are given in Table 4.8. Comparison of DE and HS by means of design criteria is given in Table 4.9. Since different design constrains are used in [61], it is not possible to perform a comparison between this work and [61]. Figures 4.19- 4.28 demonstrate that SPICE Simulator validates the DE and HS based design results as design specifications are met.

Table 4.9 Comparison of DE and HS by means of design criteria

COMPARATOR Design Criteria	**Specifications**	**DE**	**HS**
Output Capacitance (pF)	≥10	10.04	10
Slew Rate (V/μs)	≥ 10	160	160
Power Dissipation (μW)	≤ 1000	511	508
Unity Gain Bandwidth (MHz)	≥10	16.055	17.255
Gain (dB)	> 80	82.424	82.932
Vic_{min} (V)	≥-1.75	-1.6042	-1.6146
Vic_{max} (V)	≤1.75	1.6458	1.5938
CMRR (dB)	> 85	87.4715	87.8223
Propagation Delay (us)	< 2	1.165	1.111
Voff (mV)	< 60	49.191	55.571
Total Area ($x10^{-10}$ m^2)	**<5**	4.60	**4.57**

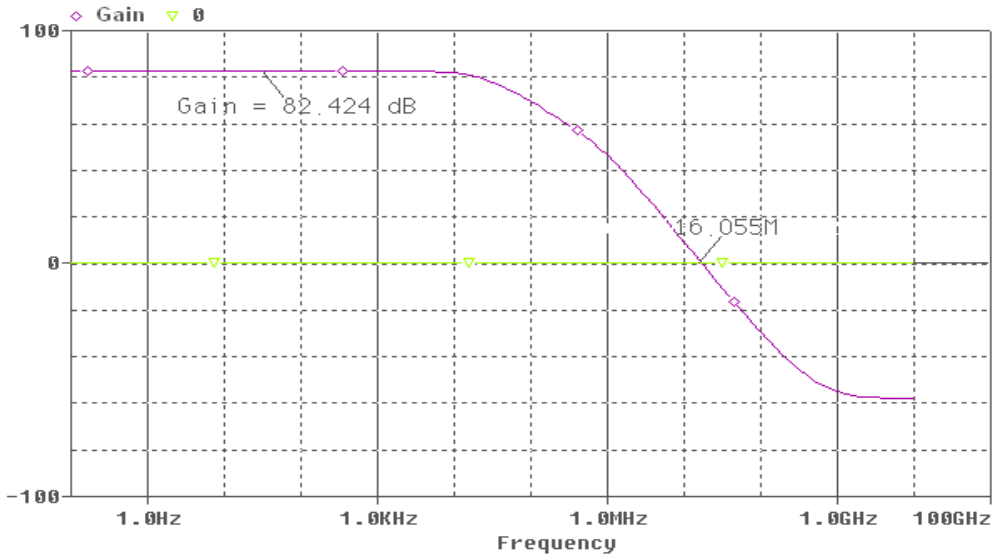

Figure 4.19 Gain of comparator with PMOS input driver designed with DE

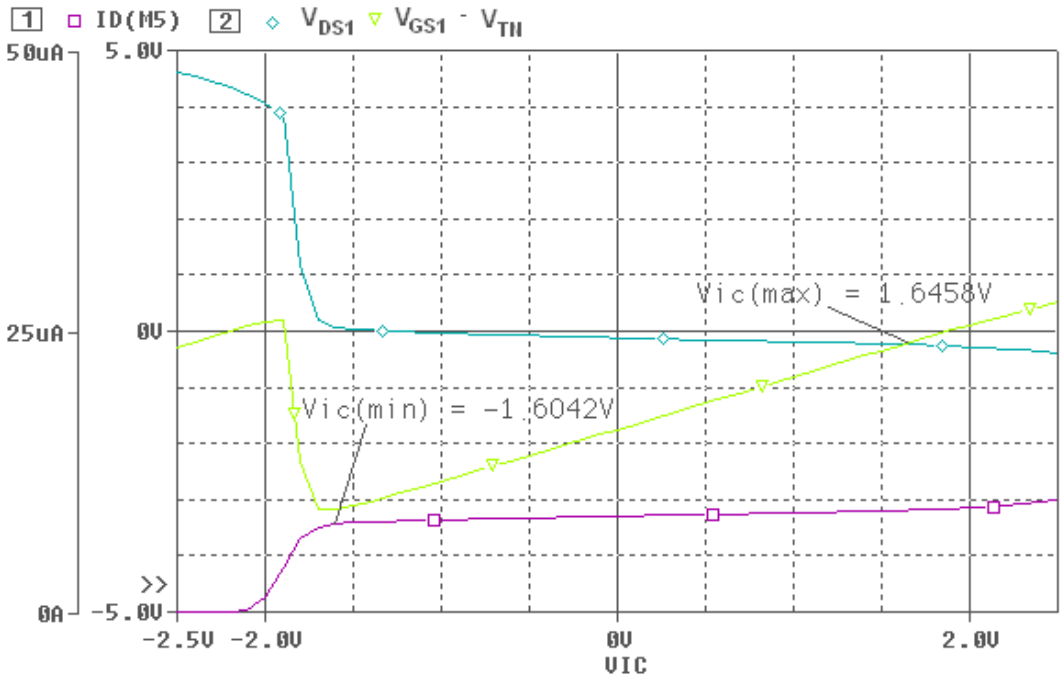

Figure 4.20 ICMR of comparator with PMOS input driver designed with DE

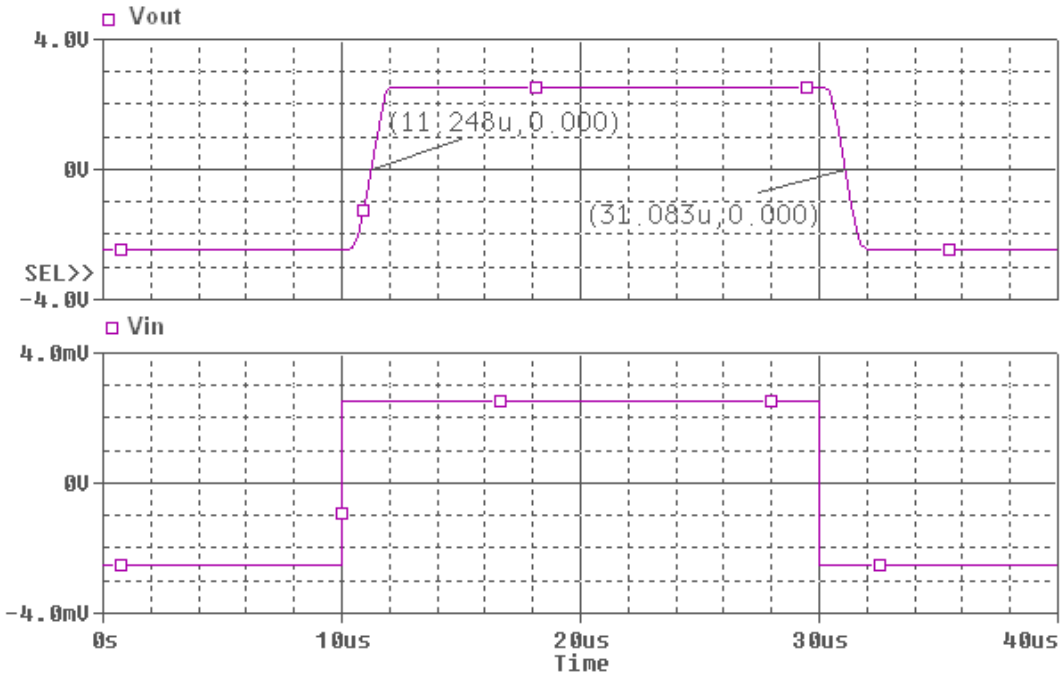

Figure 4.21 Propagation delay of comparator with PMOS input driver designed with DE

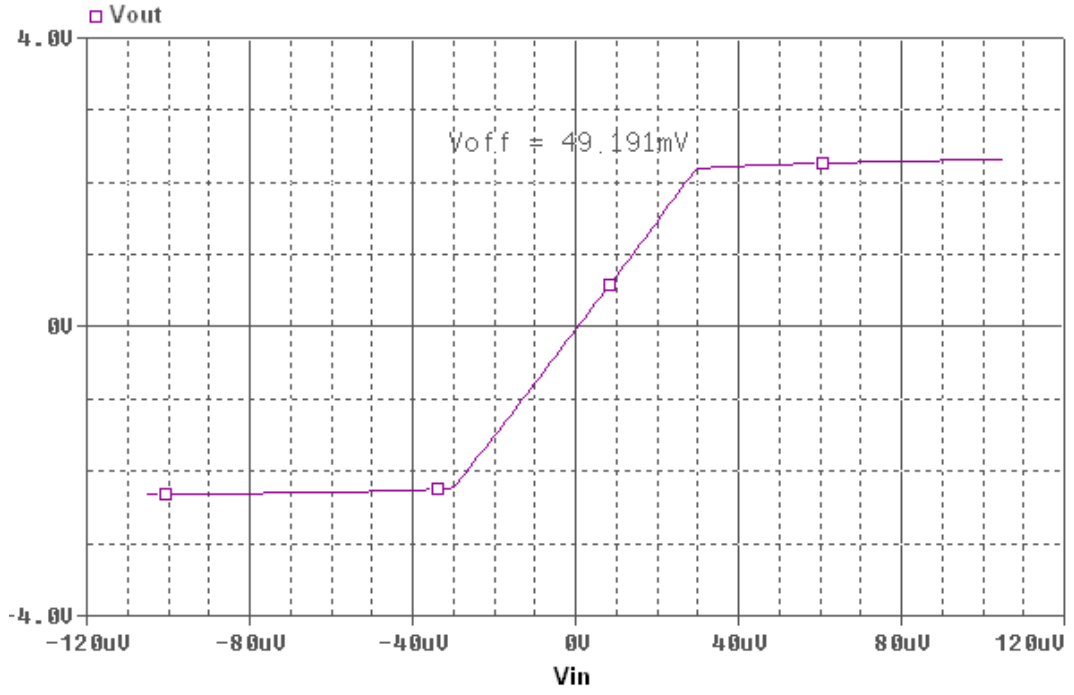

Figure 4.22 Offset voltage of comparator with PMOS input driver designed with DE

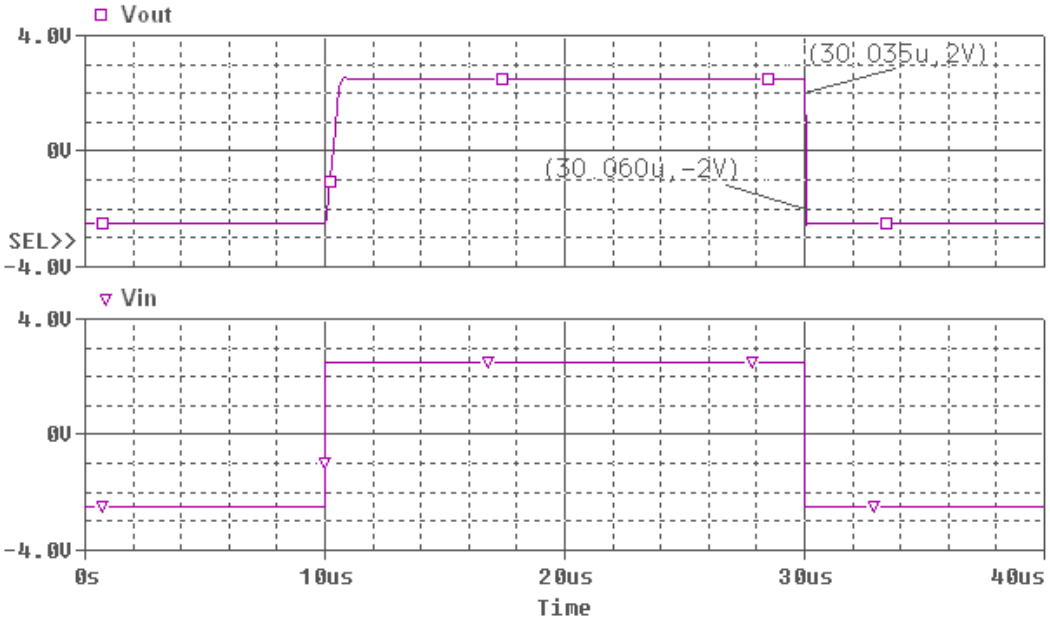

Figure 4.23 Slew rate of comparator with PMOS input driver designed with DE

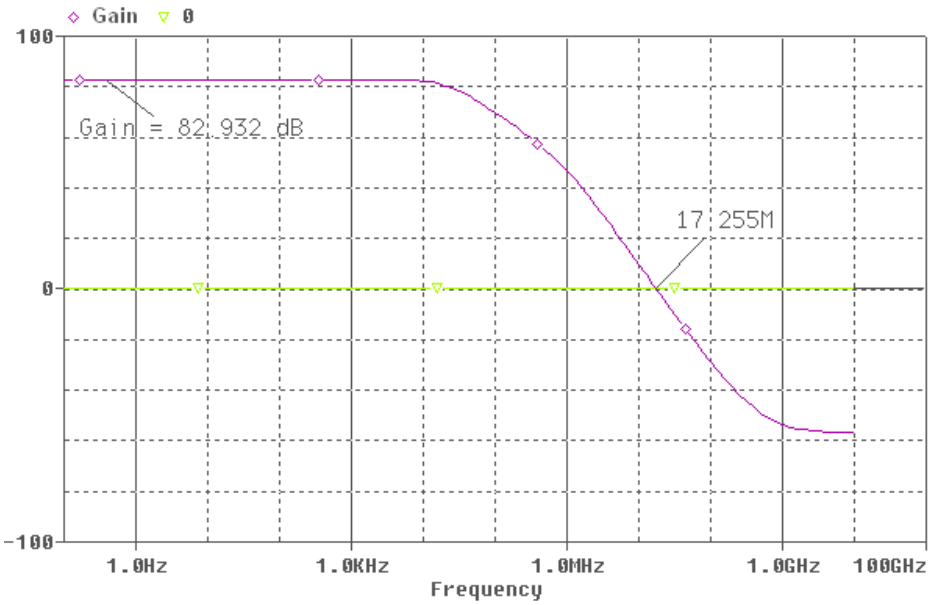

Figure 4.24 Gain of comparator with PMOS input driver designed with HS

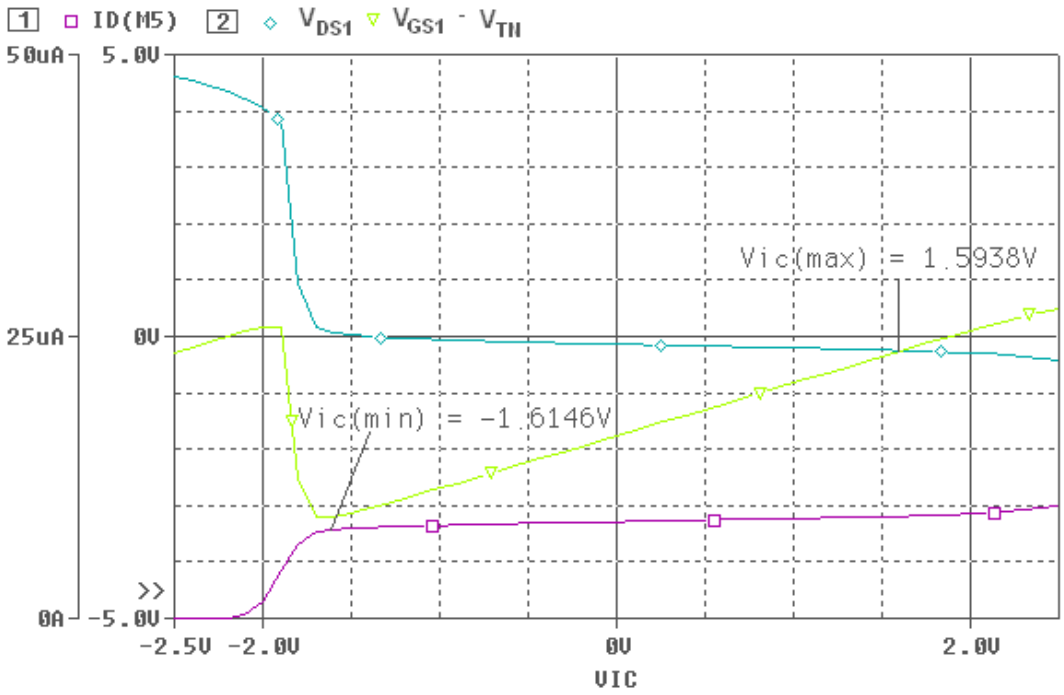

Figure 4.25 ICMR of comparator with PMOS input driver designed with HS

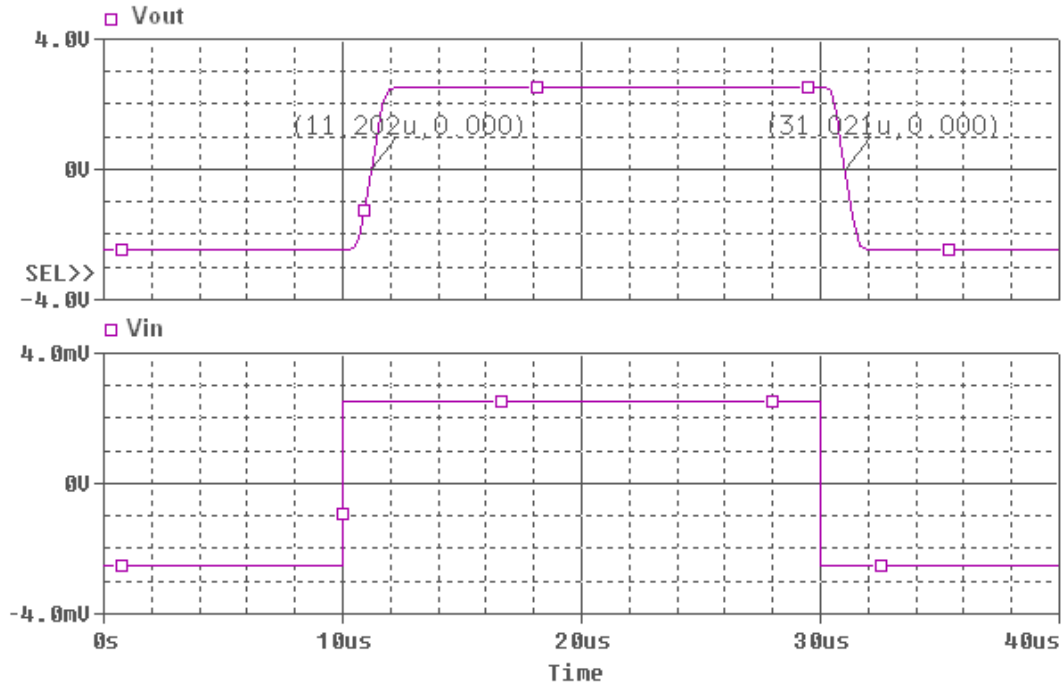

Figure 4.26 Propagation delay of comparator with PMOS input driver designed with HS

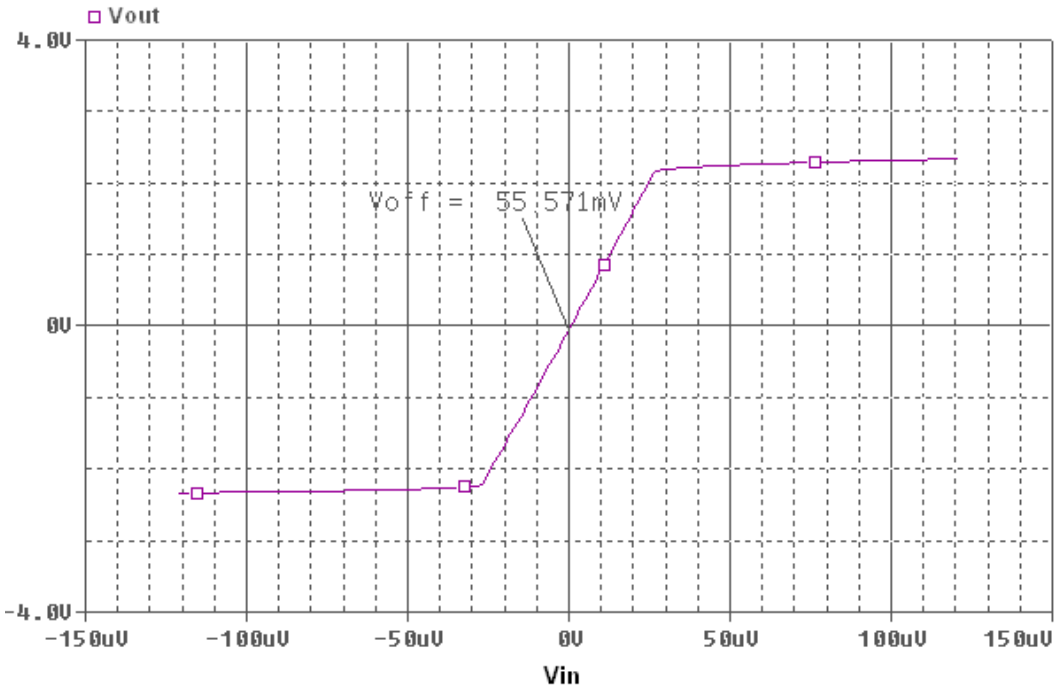

Figure 4.27 Offset voltage of comparator with PMOS input driver designed with HS

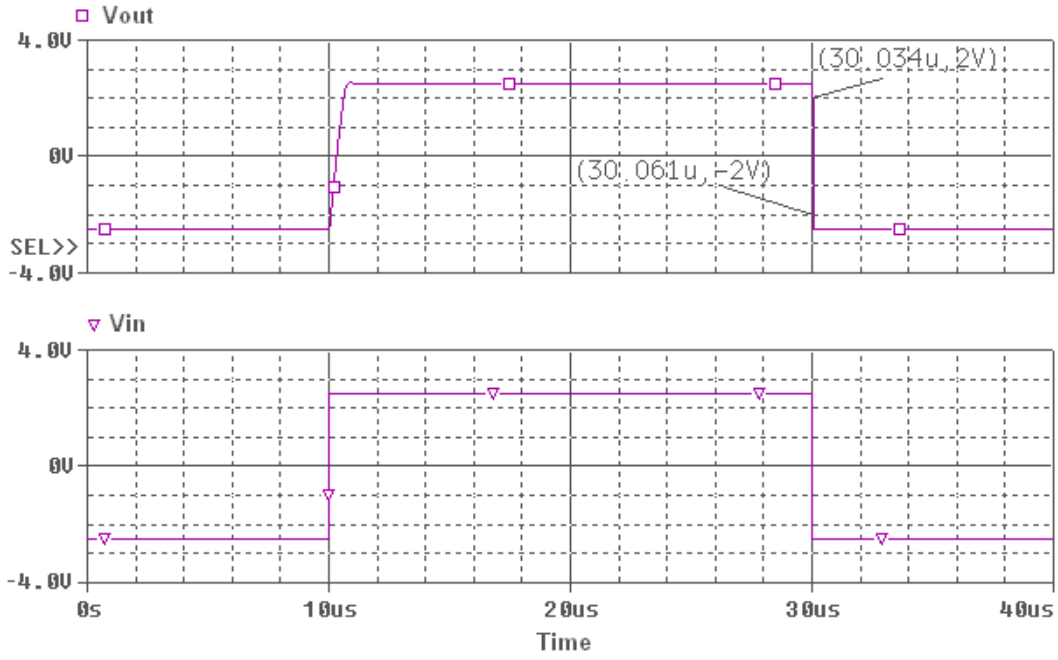

Figure 4.28 Slew rate of comparator with PMOS input driver designed with HS

4.4 Summary

In this work, particular specifications for a specified topology of a differential amplifier, operational amplifier and comparator are aimed to be met by adjusting design variables such as device sizes and bias currents by DE and HS methods. Design equations are utilized for cost function of metaheuristics, considering that numerous conflicting design criteria are of concern. Resulting design variables are utilized for redesign in SPICE simulator in order to validate the exact values of design specifications obtained with metaheuristics. Simulation results proved that DE and HS based design not only meets all design specifications but also minimizes total MOS area with respect to the previous methods. While minimum occupied MOS transistor area is obtained with HS, DE is superior in computation time and also improved ICMR and cut-off frequency with respect to HS and PSO. As further work, these methods would be investigated in mixed signal circuit optimization.

CHAPTER 5

CONCLUSION AND SUGGESTIONS

In this study, the applicability of DE and HS algorithms on the analog circuit design have been investigated. For this purpose these algorithms are utilized as an optimization tool for both discrete and integrated circuits. In chapter 3, the performances of two nature-inspired metaheuristics on analog filter design have been explored. DE and HS algorithms were utilized for both 4^{th} order Butterworth low pass filter and 2^{nd} order SVF design. Considering Butterworth filter design, both algorithms minimized the total design error with respect to previous methods. Components of SVF are selected from both E24 and E96 series in order to investigate whether performance of DE and HS will be affected when same topology is designed with different series. Considering SVF design with E24 series, DE successfully minimized the design error in a short computation time. Box and whisker plots also demonstrate that variation of CF values obtained with DE method is the smallest when multiple runs are of concern. HS obtained the minimum design error when components are selected from E96 series. Monte Carlo and worst case analysis results are also presented in order to demonstrate the robustness of the proposed approaches especially for SVF design. As a result, we are able to say that HS and DE methods are suitable for optimizing analog discrete circuits. In chapter 4, specifications for differential amplifier, operational amplifier and comparator are aimed to be met by adjusting design variables such as device sizes and bias currents by DE and HS methods. Simulation results proved that DE and HS based design not only meets all design specifications but also minimizes total MOS area with respect to the previous methods. While minimum

occupied MOS transistor area is obtained with HS, DE is superior in computation time and also improved ICMR and cut-off frequency with respect to HS and PSO.

As a further work these algorithms could be used for mixed analog circuit automation and an interface between MATLAB and SPICE could be developed in order to minimize total design time.

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APPENDIX-A

TSMC 0.35 µm MODEL PARAMETERS

```
.MODEL NMOS1 NMOS                                   LEVEL  = 7
+VERSION = 3.1            TNOM    = 27              TOX    = 7.8E-9
+XJ      = 1E-7           NCH     = 2.2E17          VTH0   = 0.4761483
+K1      = 0.6147836      K2      = 2.867694E-4     K3     = 100
+K3B     = -10            W0      = 2.600765E-5     NLX    = 2.25701E-7
+DVT0W   = 0              DVT1W   = 0               DVT2W  = 0
+DVT0    = 4.2158797      DVT1    = 0.6077768       DVT2   = -0.048051
+U0      = 358.2644557    UA      = -7.65556E-10    UB     = 2.054672E-18
+UC      = 1.641937E-11   VSAT    = 1.374794E5      A0     = 1.2164483
+AGS     = 0.1809739      B0      = 8.878483E-7     B1     = 5E-6
+KETA    = 8.10016E-4     A1      = 3.993837E-4     A2     = 0.4923356
+RDSW    = 544.6941443    PRWG    = 0.1796386       PRWB   = -0.0911284
+WR      = 1              WINT    = 1.354508E-7     LINT   = 1.454983E-9
+XL      = -5E-8          XW      = 1.5E-7          DWG    = -7.29699E-10
+DWB     = 7.151736E-9    VOFF    = -0.0672255      NFACTOR= 1.2933668
+CIT     = 0              CDSC    = 2.4E-4          CDSCD  = 0
+CDSCB   = 0              ETA0    = 0.1063985       ETAB   = -0.0141482
+DSUB    = 0.4931007      PCLM    = 2.6057248       PDIBLC1= 1.271824E-3
+PDIBLC2 = 2.180112E-3    PDIBLCB= 0.1              DROUT  = 4.431661E-4
+PSCBE1  = 7.320236E8     PSCBE2  = 1E-3            PVAG   = 9.330174E-3
+DELTA   = 0.01           RSH     = 80.4            MOBMOD = 1
+PRT     = 0              UTE     = -1.5            KT1    = -0.11
+KT1L    = 0              KT2     = 0.022           UA1    = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11        AT     = 3.3E4
+WL      = 0              WLN     = 1               WW     = 0
+WWN     = 1              WWL     = 0               LL     = 0
+LLN     = 1              LW      = 0               LWN    = 1
+LWL     = 0              CAPMOD  = 2               XPART  = 0.5
+CGDO    = 3.11E-10       CGSO    = 3.11E-10        CGBO   = 1E-12
+CJ      = 9.16922E-4     PB      = 0.8             MJ     = 0.3478704
+CJSW    = 3.291571E-10   PBSW    = 0.8             MJSW   = 0.1145248
+CJSWG   = 1.82E-10       PBSWG   = 0.8             MJSWG  = 0.1145248
+CF      = 0              PVTH0   = -0.0139075      PRDSW  = -47.7936722
+PK2     = 2.359942E-3    WKETA   = 6.320378E-4     LKETA  = -4.325395E-3
```

```
.MODEL PMOS1 PMOS                                   LEVEL   = 7
+VERSION = 3.1           TNOM    = 27             TOX     = 7.8E-9
+XJ      = 1E-7          NCH     = 8.52E16        VTH0    = -0.6513775
+K1      = 0.4286847     K2      = -5.542793E-3   K3      = 97.1641761
+K3B     = -5            W0      = 7.054287E-6    NLX     = 2.516648E-7
+DVT0W   = 0             DVT1W   = 0              DVT2W   = 0
+DVT0    = 1.7876132     DVT1    = 0.5369794      DVT2    = 3.747654E-3
+U0      = 149.2330772   UA      = 1E-10          UB      = 1.535287E-18
+UC      = -2.41558E-11  VSAT    = 1.540022E5     A0      = 0.7990549
+AGS     = 0.2670643     B0      = 2.609264E-6    B1      = 5E-6
+KETA    = -3.612338E-3  A1      = 2.72138E-4     A2      = 0.9725641
+RDSW    = 3.156499E3    PRWG    = -0.1013163     PRWB    = 0.0728675
+WR      = 1             WINT    = 1.342653E-7    LINT    = 0
+XL      = -5E-8         XW      = 1.5E-7         DWG     = -9.772747E-9
+DWB     = 1.491485E-8   VOFF    = -0.122767      NFACTOR= 1.9970207
+CIT     = 0             CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.099556       ETAB    = 2.606693E-3
+DSUB    = 0.6275991     PCLM    = 5.5082963      PDIBLC1= 9.987419E-4
+PDIBLC2 = 0.0117981     PDIBLCB= 0.1             DROUT   = 3.141427E-6
+PSCBE1  = 8E10          PSCBE2 = 5.027754E-10    PVAG    = 9.6519816
+DELTA   = 0.01          RSH     = 154.6          MOBMOD = 1
+PRT     = 0             UTE     = -1.5           KT1     = -0.11
+KT1L    = 0             KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0             WLN     = 1              WW      = 0
+WWN     = 1             WWL     = 0              LL      = 0
+LLN     = 1             LW      = 0              LWN     = 1
+LWL     = 0             CAPMOD = 2               XPART   = 0.5
+CGDO    = 4.08E-10      CGSO    = 4.08E-10       CGBO    = 1E-12
+CJ      = 1.413322E-3   PB      = 0.99           MJ      = 0.5609267
+CJSW    = 2.978864E-10  PBSW    = 0.99           MJSW    = 0.3817474
+CJSWG   = 4.42E-11      PBSWG   = 0.99           MJSWG   = 0.3817474
+CF      = 0             PVTH0   = 7.800191E-3    PRDSW   = 29.6696742
+PK2     = 2.25328E-3    WKETA   = -4.072642E-5   LKETA   = -6.119295E-3
```

CURRICULUM VITAE

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Name and Surname : Ufuk BOZKURT

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EDUCATION LEVEL

Degree	Department	School/University	Year of Graduation
Undergraduate Education	Electrical and Electronics Engineering	Istanbul University	2008
High School	Natural and Applied Sciences	Bahçelievler Foreign Language Intensive High School	2004

WORK EXPERIENCE

Year	Firm/Corporation	Job
2008 - Still	NETAŞ	Senior Engineer
2007 - 2008	Pozitim Technology	Junior Project Manager