

YILDIZ TEKNİK ÜNİVERSİTESİ * FEN BİLİMLERİ ENSTİTÜSÜ

Cpc 464 Amstrad için Ram Disc

Fatih Şimşek

Yüksek Lisans Tezi

YILDIZ ÜNİVERSİTESİ
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YILDIZ ÜNİVERSİTESİ

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YILDIZ ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ

Amstrad CPC 464 bilgisayarını için RAM DISC konulu
çalışmada proje kurmuş ve düzen ve yönlendiren değerli
öğretimin için teşekkür ederim.

CPC 464 AMSTRAD BİLGİSAYARI İÇİN RAM DISC

YÜKSEK LİSANS TEZİ
MÜH. FATİH ŞİMŞEK

İSTANBUL-1988

Ö N S Ö Z

Amstrad CPC 464 bilgisayarı için RAM DISC konulu çalışmamda proje konusunu öneren ve yönlendiren değerli Öğretim Üyesi Sayın Doç. Dr. Sezgin ALSAN'a teşekkür ederim.

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Ö Z E T

Projenin amacı Amstrad CPC 464 Bilgisayarı için Ram Disc gerçekleştirmektir. Her biri 8KByte olan 6264LP ran'ları ile 32K-Byte'lık Disc Memory sağlanmıştır. Ram Disc'e Basic bölgesinden 4 ayrı program , bir isim altında kaydedilebilir. Disc'de mevcut programlar isim belirterek, Basic'e transfer edilebilir veya silinebilir..

S U M M A R Y

The aim of this project is to realised Ram Disc to AMSTRAD CPC 464 computer. Disc memory has been expanded to 32KByte by using of 8KByte 6264LP Ram chips each. Four different program from Basic area can be entered to Ram Disc with under a name. The program which are in the Disc may be either transfered to Basic and erased.

veyr sürüşdür.

Bu model 311 ayarlı tip monitöre bağlanabilir. Bun-
lardan birincisi 27 64/65 model yeşil tüplü monitör,
ikincisi ise CTC 992 modeli renkli monitördür.

CPC 464 2-80 A mikroisleyicisi bulunur. Bu
mikroisleyicinin saat frekansı 4 MHz. hercadığı gnc ise
1800 mdir. 8 bitlik bu mikroisleyicinin yazılım ta-
hantı çok güçlüdür. Bu da ona oldukça geniş bir program
destek sağlamaktadır.

Farklı Modlar

Amstrad CPC 464 bilgisayarlarında 3 farklı ek-
ran moduna geçiş yapılabilir. Bunlar Mod 1 ve
Mod 2 dir.

Mod 0 (Mode 0)

Bu modda 20 sütun ve 25 satırdan oluş-
tur. Ekrandaki bir satıra en fazla 20 karakter yazı-
labılır. 16 renk olanağı vardır.

Mod 1 (Mode 1)

Bu modda 40 sütun ve 25 satırdan oluş-
tur. Ekrandaki bir satıra en fazla 40 karakter yazı-
labılır. 4 renk olanağı vardır.

Mod 2 (Mode 2)

Bu modda 80 sütun ve 25 satırdan oluşur.
Ekrandaki bir satıra en fazla 80 karakter yazılabilir.
2 renk olanağı vardır.

AMSTRAD CPC 464 BİLGİSAYARININ TANITIMI

- CPC 464'de 64 kilobayt dinamik RAM, vardır. ve teyp sürücülüdür.

Bu model iki ayrı tip monitöre bağlanabilir. Bunlardan birincisi GT 64/65 model yeşil tüylü monitör, ikincisi ise CTM 640 modeli renkli monitördür.

CPC 464'de Z-80 A mikroişleyicisi bulunur. Bu mikroişleyicinin saat frekansı 4 MHZ harcadığı güç ise 1000 mW'dır. 8 bit'lik bu mikroişleyicinin yazılım tabanı çok güçlüdür. Bu da ona oldukça geniş bir program desteği sağlamaktadır.

Ekran Mod'ları

Amstrad CPC 464 bilgisayarlarında 3 farklı ekran mod'unda çalışma imkanı vardır. Bunlar Mod 1 ve Mod 2 dir.

Mod 0 (Mode 0)

Ekran bu mod'da 20 sütun ve 25 satırdan oluşur. Ekrandaki bir satıra en fazla 20 karakter yazılabilir. 16 renk olanağı vardır.

Mod 1 (Mode 1)

Ekran bu mod'da 40 sütun ve 25 satırdan oluşur. Ekrandaki bir satıra en fazla 40 karakter yazılabilir. 4 renk olanağı vardır.

Mod 2 (Mode 2)

Ekran bu mod'da 80 sütun ve 25 satırdan oluşur. Ekrandaki bir satıra en fazla 80 karakter yazılabilir. 2 renk olanağı vardır.

BELLEK HARİTASI DÜZENİ

CPC 464 bilgisayarın 64 kilobayt'lık bellek alanı aşağıda görüldüğü gibi belirli bölgelere ayrılmıştır.

	0 0 0 0	H			
ROMO	3 F F F	H	16 K	ROM ve RAM	çakışık
	4 0 0 0	H			
			16 K	RAM	
	7 F F F	H			
	8 0 0 0	H			
			16 K	RAM	
	B F F F	H			
ROM 1	C 0 0 0	H			
			16 K	ROM ve ekran RAM	çakışık
	F F F F	H			

GİRİŞ/ÇIKIŞ HARİTASI DÜZENİ (I/O)

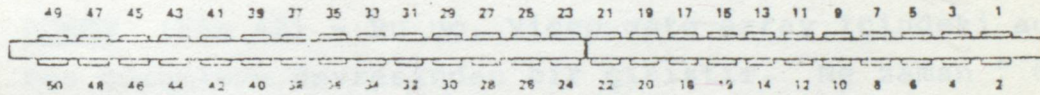
Amstrad CPC 464 bilgisayarına yapılacak olan herhangi bir arabilim, ancak bu bilgisayarın belirli bir giriş/çıkış adresine yerleştirilebilir. Kullanıcıya serbest olarak bırakılan bu adres bölgeleri şunlardır.

F8E0 ... F8FF	H	32 bayt
F8E0 ... F8FF	H	" "
F9E0 ... F9FF	H	" "
FAE0 ... FAFF	H	" "
FBE0 ... FBFF	H	" "

Toplam 128 bayt'lık bir giriş çıkış adresi kullanıcıya bırakılmıştır. Kullanıcı kendi isteği doğrultusunda bu adreslerden birini veya daha fazlasını seçebilir.

GENİŞLEME İÇİN GİRİŞ/ÇIKIŞ PORTU

Amstrad CPC 464 bilgisayarlarına ait her klavyenin arkasında 2 x 25 yollu bir genişleme port'u bulunur. Bu port'a disk sürücüsü veya seri haberleşmeyi sağlayan bazı özel arabirimler bağlanabilir. Tez çalışmasında gerçekleştirilen RAMDISC devresi de bu port'a bağlanmıştır. Şekil de genişleme portu'nun arkadan görünüşü ve uç tanımlamaları görülmektedir.



PIN 1	SOUND	PIN 18	A0	PIN 35	$\overline{\text{INT}}$
PIN 2	GND	PIN 19	D7	PIN 36	$\overline{\text{NMI}}$
PIN 3	A15	PIN 20	D6	PIN 37	$\overline{\text{BUSRD}}$
PIN 4	A14	PIN 21	D5	PIN 38	$\overline{\text{BUSAK}}$
PIN 5	A13	PIN 22	D4	PIN 39	$\overline{\text{READY}}$
PIN 6	A12	PIN 23	D3	PIN 40	$\overline{\text{BUS RESET}}$
PIN 7	A11	PIN 24	D2	PIN 41	$\overline{\text{RESET}}$
PIN 8	A10	PIN 25	D1	PIN 42	$\overline{\text{ROMEN}}$
PIN 9	A9	PIN 26	D0	PIN 43	$\overline{\text{ROMDIS}}$
PIN 10	A8	PIN 27	+5v	PIN 44	$\overline{\text{RAMRD}}$
PIN 11	A7	PIN 28	$\overline{\text{MREQ}}$	PIN 45	$\overline{\text{RAMDIS}}$
PIN 12	A6	PIN 29	$\overline{\text{M1}}$	PIN 46	$\overline{\text{CURSOR}}$
PIN 13	A5	PIN 30	$\overline{\text{RFSH}}$	PIN 47	$\overline{\text{L. PEN}}$
PIN 14	A4	PIN 31	$\overline{\text{IORQ}}$	PIN 48	$\overline{\text{EXP}}$
PIN 15	A3	PIN 32	$\overline{\text{RD.}}$	PIN 49	GND
PIN 16	A2	PIN 33	$\overline{\text{WR}}$	PIN 50	ϕ
PIN 17	A1	PIN 34	HALT		

Expansion bus'un bir çok sinyali, Z80A microprocessordan direkt olarak alınır. CPC'nın özel signal'leri ve onların fonksiyonları aşağıda açıklanmıştır.

BUS RESET (Pin 40) - Bu uç, harici bir switch bağlantısı için bir giriştir. Bu switch BUSRESET ucu ile GROUND (Pin 2,49,63 veya 64) arasına bağlanmalıdır. Switch'e basıldığında computer reset olur, switch ilk konumuna döndüğünde CPC power on yapılmış gibi restart olur.

RESET (Pin 41) - Bu uç, CPC içindeki Power On Circuit (POR)'den bir çıkıştır. Expansion bus'a bağlanacak devrelerdeki tüm devrelerin reset girişlerine bağlanabilir.

ROMEN (Pin 42) - Bu uç, Video gate array içindeki adres çözümleme devresinden bir çıkıştır. Ne zaman "0" a giderse, adres hattı içeriği Upper ROM için uygulanabilir bir adres - niteliğindedir- Adres aralığı 0000 den FFFF'e kadardır.

ROMDIS (Pin 43) - Bu uç, CPC içindeki ROM chip'i "1" aldığı anda, bir giriş ucudur. ROM chip tamamıyla devre dışı olana kadar, lower ve upper ROM'larının her ikisinin de parçalarına erişilemeyecektir.

RAMRD (Pin 44) - Bu çıkış "0" a gittiğinde, bilgi hattı ile CPC RAM arasındaki Video gate array buffer'ı açılır. Diğer bir deyişle, bu çıkış "0" a gittiğinde Z80A RAM'dan bilgi okur.

CURSOR (Pin 46) - HD6845 VDU controller chip'i üzerindeki cursor enable ucuna bağlanmalıdır.

LPEN (Pin 47) - Bu uç, Light pen'e bağlantı yapmak için bir giriştir.

EXP (Pin 48) - Bu girişin işlevi, Amstrad hardware dokümanlarında açıkça tanımlanmamıştır. 8255A PPI chip'inin Port B' sinin 5 bit'ine bağlanmalıdır.

İşlevsel Tanımlar

Veri Hattı Bufferi (Data Bus Buffer) : Bu bu konumda, biddirectional 8 bit girişli, 8255 A ya bağlı veri hattına uygulanır. Bilgi akışı CPU giriş ve ya çıkış konumlarıyla olabilir veya verilir. Kontrol ve bilgileri de, bilgi hattı buffer üzerinden transfer edilir.

Read/Write ve Kontrol Çıkışı : Bu çıkış konumunda, Read/Write ve Kontrol Çıkışı olarak her ikisinin de bilgileri ve harici CPU transferlerini kullanmaktadır.

Chip Select : Bu uç "aktif" iken, bu giriş arca 8255A ve CPU arasında haberleşmeyi mümkün kılar.

8255 A

(Programmable Peripheral Interface)

Genel amaçlı, programlanabilir 8255 A I/O devresi Intel firmasınınca dizayn edilmiştir. 8255, 24 adet; 12 nin 2 li grupları halinde teker teker programlanabilir ve üç önemli çalışma modun da kullanılabilen I/O ucuna sahiptir. İlk modda, (MODE 0) 12 I/O ucunun her grubu, 4'lü olarak giriş veya çıkış olarak programlanabilir. İkinci modda (MODE 1) her grup 8 hat olarak, giriş veya çıkış olarak programlanabilir. Kalan 4 ucun üçü anlaşma (Handshaking) ve kontrol sinyal'leri için kullanılır. Üçüncü çalışma modunda, (MODE 2) diğer grupdan anlaşma için 5 hattı ödünç alan ve "bidirectional bus" için 8 hat kullanan, çalışma modudur.

İŞLEVSEL TANIMLAR

Veri hattı sürücüsü (Data Bus Buffer) : Bu üç konumlu, bidirectional 8 bit sürücü, 8255 A yı sistem veri hattına uygunlaştırır. Bilgi sürücü üzerinde CPU giriş veya çıkış komutlarıyla alınır veya verilir. Kontrol ve bilgileri'de, bilgi hattı sürücüsü üzerinden transfer edilir.

Read/Write ve Kontrol lojik : Bu bloğun fonksiyonu Bilgi, Kontrol ve durum kelimelerinin her ikisinin dahili ve harici tüm transferlerini kullanmaktır.

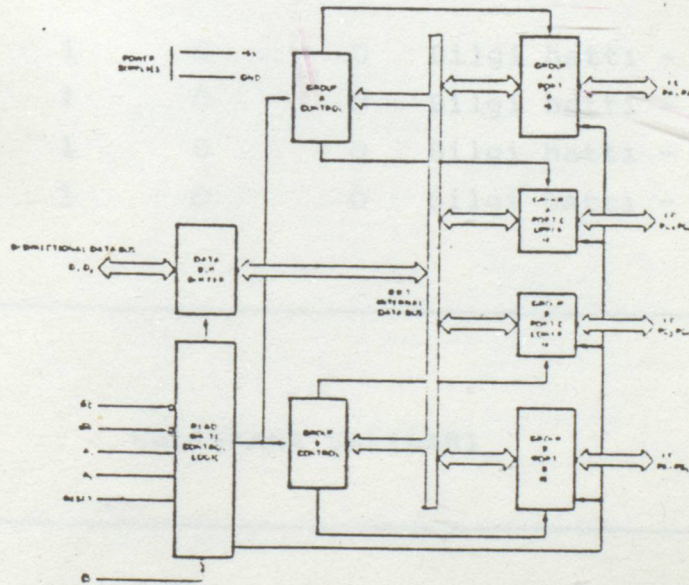
(CS) Chip select : Bu uç "sıfır" iken, bu giriş ucu 8255A ve CPU arasında haberleşmeyi mümkün kılar.

(RD) Read : Read ucu "sıfır" iken, bu giriş ucu 8255 A dan CPU'ya bilgi hattı üzerinden Bilgi veya durum bilgisi yollamak için kullanılır. Esas olarak CPU'nun izniyle 8255 A tarafından okunur.

(WR Write : Write ucu "sıfır" iken, bu giriş ucu CPU'yu 8255 A'ya Kontrol veya Bilgi kelimeleri yazmasını mümkün kılar.

(A₀ ve A₁) : Bu giriş sinyalleri RD veya WR girişlerinin birlikte kullanılmasıyla üç port'un birinin veya "Control word yazmacı" nın seçilmesinin kontrolünü yapar. Bu uçlar, adres hattının A₀ ve A₁ bit'ine normal olarak bağlanabilir.

Not olarak; 8255 A, MODE 1 veya MODE 2 de çalışmaya programlandığında CPU'ya kesinti isteği sinyalleri gibi kullanılabilir. "kontrol sinyal"leri sağlar. Bu kesinti isteği sinyalleri Port C'den üretilir.



8255 A BLOK DİYAGRAMI

GİRİŞ ÇALIŞMASI

A1	AO	$\overline{RD}$	$\overline{WR}$	CS	(READ)
0	0	0	1	0	PORT A - Bilgi hattı
0	1	0	1	0	PORT B - Bilgi hattı
1	0	0	1	0	PORT C - Bilgi hattı

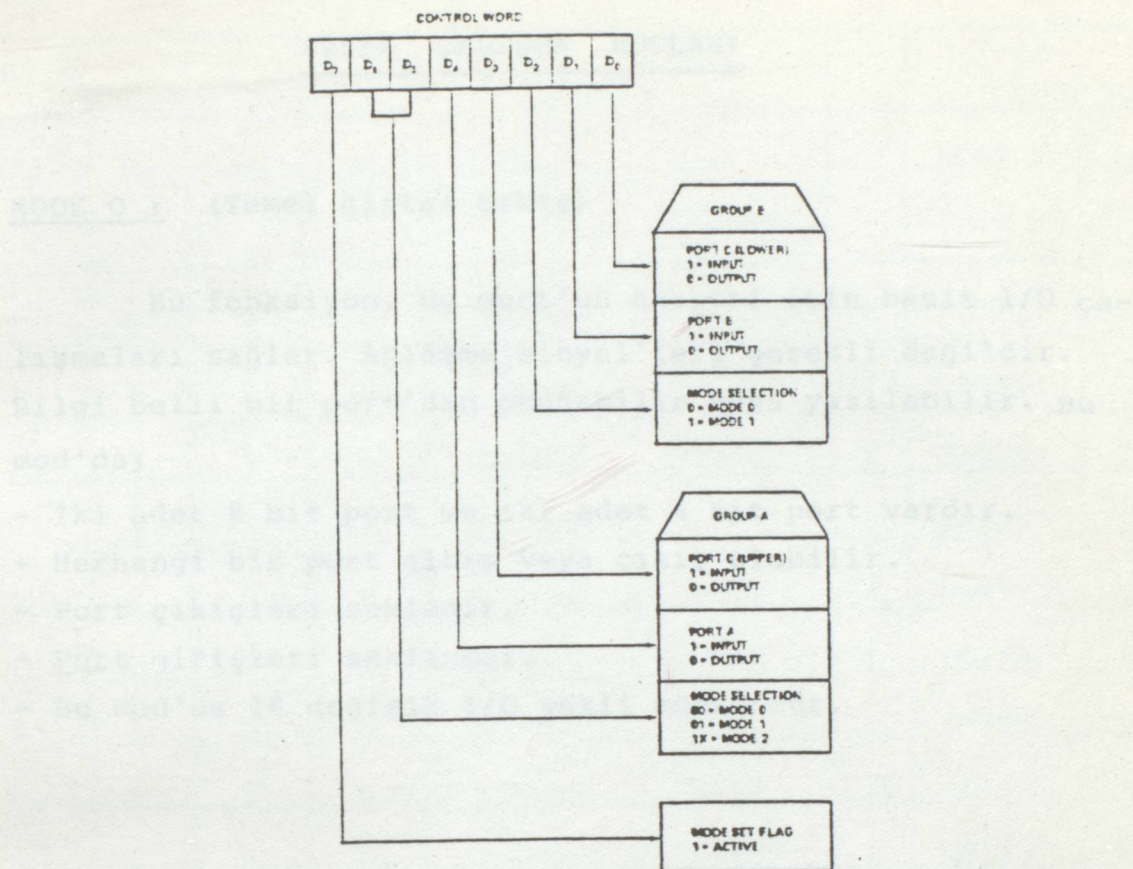
ÇIKIŞ ÇALIŞMASI

(WRITE)

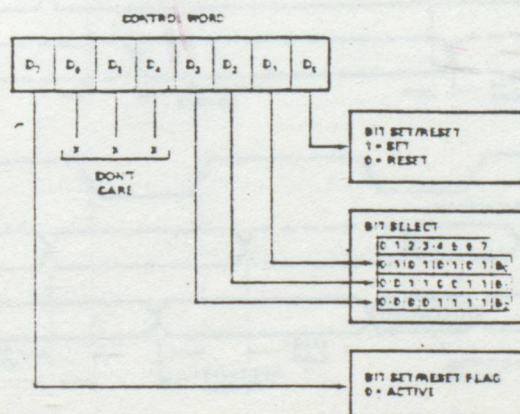
0	0	1	0	0	Bilgi hattı - PORT A
0	1	1	0	0	Bilgi hattı - PORT B
1	0	1	0	0	Bilgi hattı - PORT C
1	1	1	0	0	Bilgi hattı - KONTROL

ÇALIŞMAMA ŞARTLARI

X	X	X	X	1	Bilgi hattı - 3 konumlu
1	1	0	1	0	Tanımsız
X	X	1	1	1	Bilgi hattı - 3 konumlu



MODE TANIMLAMA ŞEKLİ



Bit Set/Reset Format

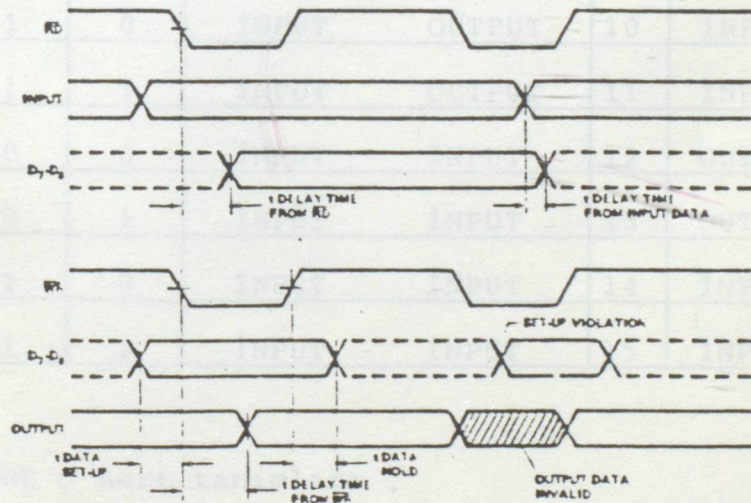
BİT SET-RESET ŞEKLİ

8255A ÇALIŞMA MODLARI

MODE 0 : (Temel giriş/ çıkış)

Bu fonksiyon, üç port'un herbiri için basit I/O çalışmaları sağlar. Anlaşma sinyal'leri gerekli değildir. Bilgi belli bir port'dan okunabilir veya yazılabilir. Bu mod'da;

- İki adet 8 bit port ve iki adet 4 bit port vardır.
- Herhangi bir port giriş veya çıkış olabilir.
- Port çıkışları saklanır.
- Port girişleri saklanmaz.
- Bu mod'da 16 değişik I/O şekli mümkündür.



MODE 0 ZAMANLAMASI

A		B		GROUP A			GROUP B	
D ₄	D ₃	D ₁	D ₀	PORT A	PORT C (UPPER)		PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 port tanımları .

Control word = 4

Data Bus = 22

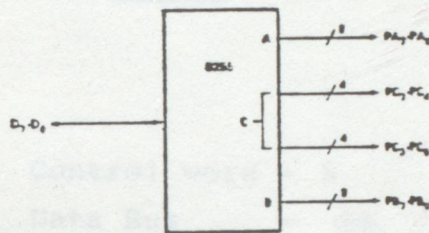
Control word = 5

Data Bus = 22

MODE 0 I/O ŞEKİLLERİ

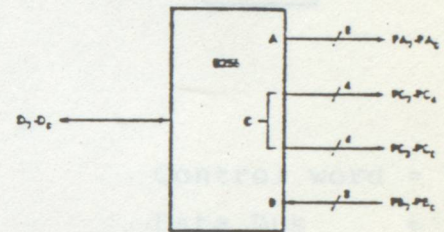
Control word = 0

Data Bus = 80



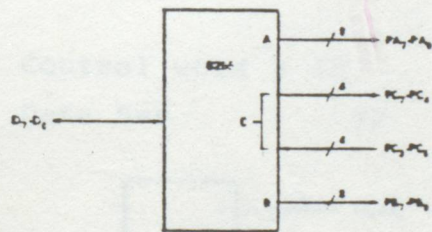
Control word = 1

Data Bus = 81



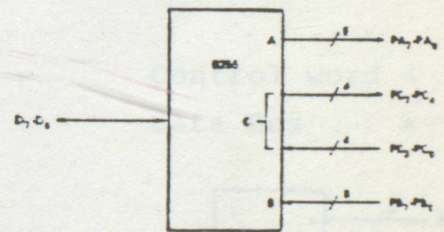
Control word = 2

Data Bus = 82



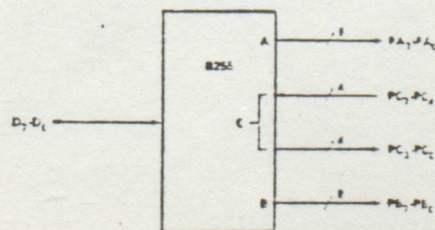
Control word = 3

Data Bus = 83



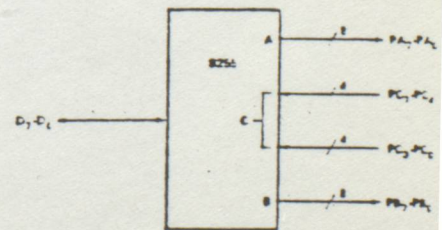
Control word = 4

Data Bus = 88

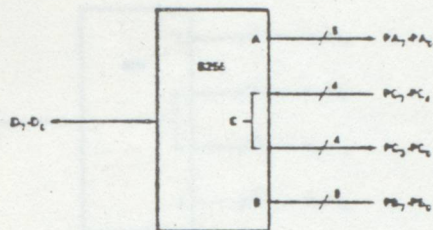


Control word = 5

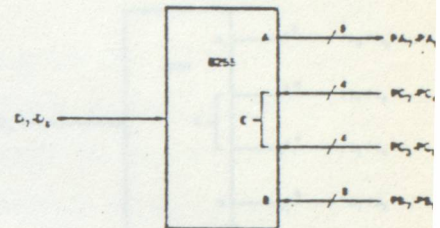
Data Bus = 89



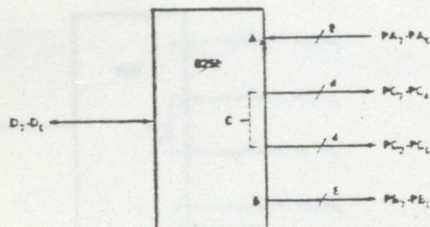
Control word = 6
Data Bus = 8A



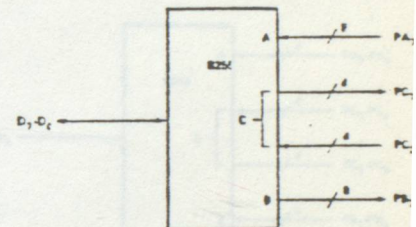
Control word = 7
Data Bus = 8



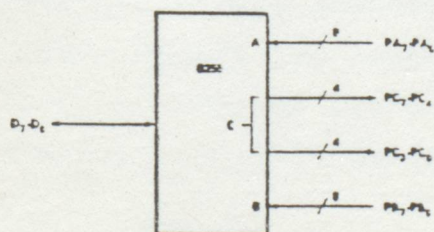
Control word = 8
Data Bus = 90



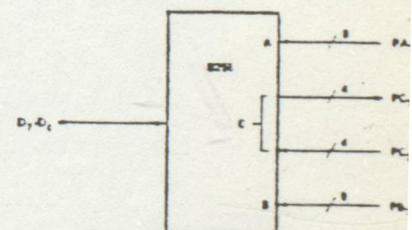
Control word = 9
Data Bus =



Control word = 10
Data Bus = 92

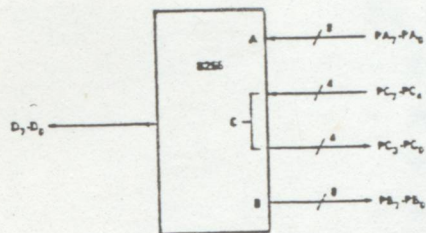


Control word = 11
Data Bus =



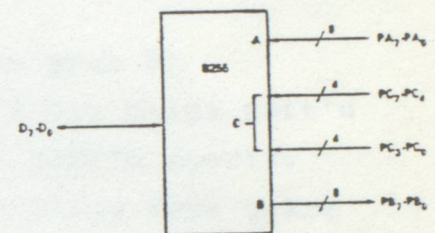
Control word = 12

Data Bus = 98



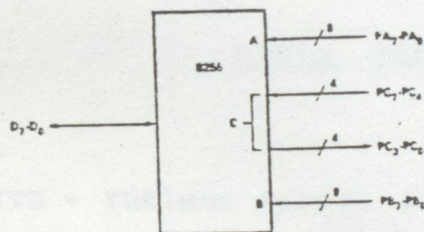
Control word = 13

Data Bus = 99



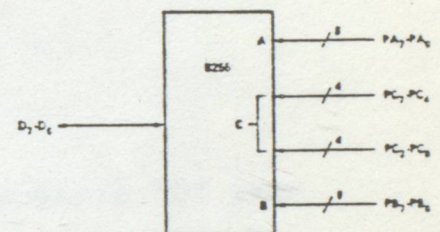
Control word = 14

Data Bus = 9A



Control word = 15

Data Bus = 9B



MODE 1 :

Bu çalışma şekli bir anlamda belli bir port'dan anlařma sinyal'lerinin veya I/O bilgisinin transferini saęlar.

Bu modda;

- İki grub (Grub A ve grub B)
- Her grub bir adet 8 bit bilgi port'u ve bir 4 bit bilgi port'u ięerir.
- 8 bit bilgi port'u giriř veya ęıkıř olabilir.
- 4 bitlik port, 8 bit bilgi port'un durum ve Kontrolü ięin kullanılmıřtır.

Giriř kontrol sinyalleri

- STB - Yükleme giriři (strobe input) : Bu giriř "0" iken giriř tutucularına bilgi yüklenir.
- IBF - Giriř tamponu dolu (Input buffer full) : Bu giriř "1" iken giriř tutucularına yüklenen bilgi, esas bilgidir. 20 giriřinin ęıkan kenarıyla; IBF , 1 , STB 0 ve reset olur.
- INTR - Kesinti isteęi (Interrupt request) : Bu ęıkıř $\overline{RD}$ düşen kenarı ile reset olur.
- INTE A - PC₄'ün set/reset bit'inin kontrolü
- INTE B - PC₂'nin set/reset bit'inin kontrolü

Çıkıř kontrol sinyalleri

- OBF - Çıkıř tamponu dolu (Output buffer full) : OBF ęıkıřı "0" 'a gidince CPU'dan ęıkan bilgi, belirlenmiř port'un ęıkıřlarından yazılır. OBF - WR giriřinin

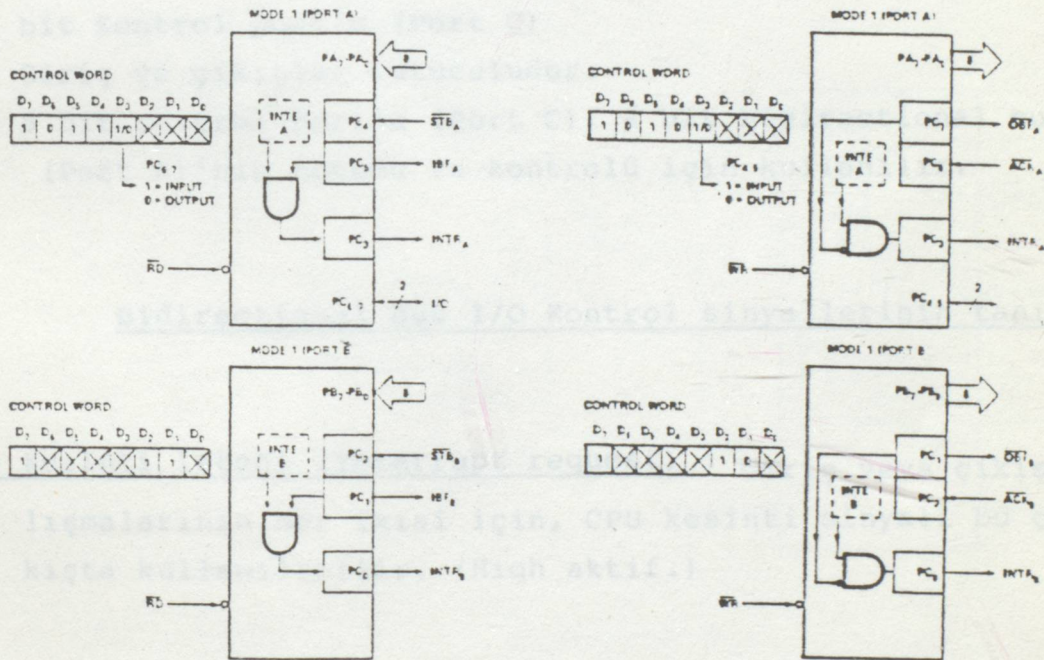
çıkan kenarı ile "1", ACK girişinin "0" olması ile reset olur.

ACK - Bilgi girişi (Acknowledge input) : Bu giriş "0" iken 8255A port A veya port B den kabul edilmiş bilgiyi verir.

INTR - Kesinti İsteği (Interrupt request) : Bu çıkış, WR işaretinin yükselen kenarıyla reset olur.

INTE A - PC₆'nın bit set/reset'i ile kontrol edilir.

INTE B - PC₂'nin bit set/reset'i ile kontrol edilir.



MODE 1 GİRİŞ

MODE 1 ÇIKIŞ

MODE 2 :

Bu çalışma şekli bir anlamda, bir çevre birimiyle her iki yönde bilgi iletimini sağlayan 8 bit'lik hat yoluyla haberleşmeyi sağlar.

Anlaşma sinyalleri, MODE 1'deki kesinti üretilmesi enable/disable fonksiyonlarına benzer bir tarzda, özel bir hat üzerinden düzenli bir akış sürdürerek sağlanır.

Bu modda;

- Yalnızca grup A kullanılır.
- Bir 8 bit bidirectional bus port'u (Port A) ve bir 5 bit Kontrol port'u (Port C)
- Giriş ve çıkışlar tutuculudur.
- 5 bit control port'u (Port C), 8 bit bidirectional bus (Port A)'nın durumu ve kontrolü için kullanılır.

Bidirectional bus I/O Kontrol sinyallerinin tanımları

INTR- Kesinti isteği (Interrupt request) : Giriş veya çıkış çalışmalarının her ikisi için, CPU kesinti sinyali bu çıkışta kullanılabilir. (High aktif.)

Output Operations

OBF- Çıkış tamponu dolu (Output buffer full) : Bu çıkış; CPU Port A'ya bilgi yazacağında "0"'a gidecektir..

ACK_Bilgi girişi (Acknowledge) : Bu giriş "0" olduğunda Port A'nın üç konumlu çıkış sürücülerinden bilgi yollanmasına izin verecektir. Aksi halde çıkış sürücüleri high impedance konumunda olacaktır.

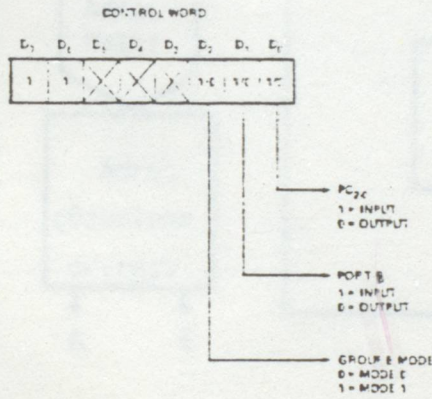
INTE 1 : PC₆'nın bit set/reset'i ile kontrol edilir.

Giriş çalışmaları

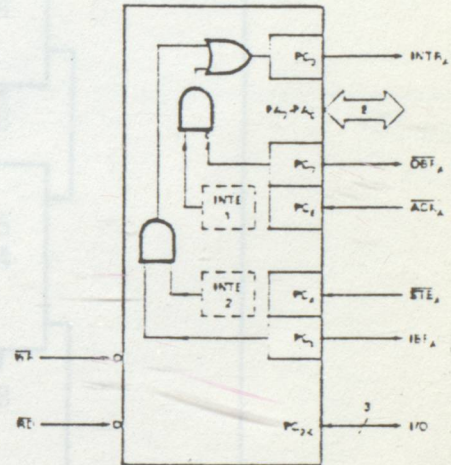
STB - İzin verme girişi (Strobe input) : Bu giriş "0" iken bilgi, girişi tutucularına yüklenir.

IBF - Giriş tamponu dolu (Input buffer full) : Bu çıkışta "1" belirdiğinde bilgi, giriş tutucularına yüklenmiştir.

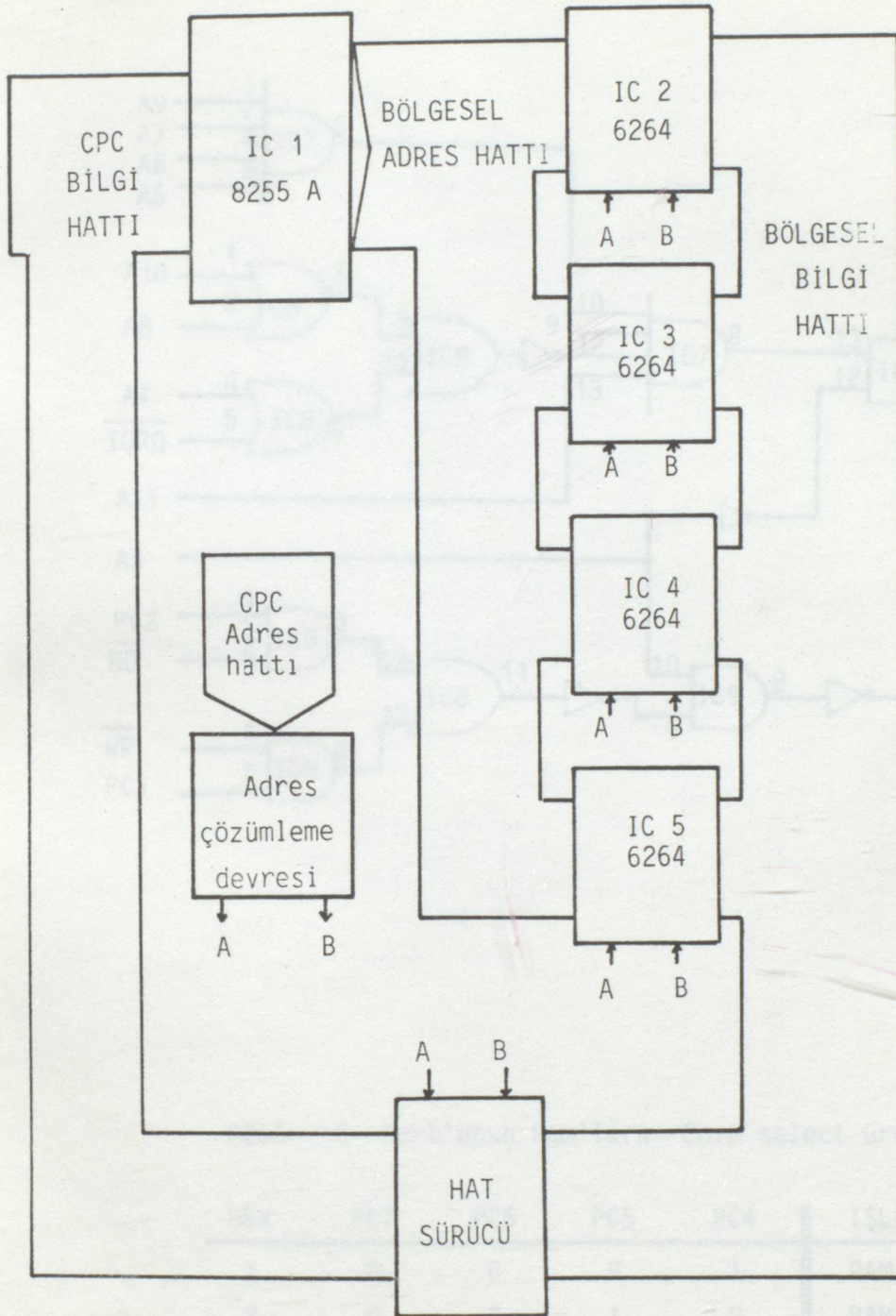
INTE 2 : PC₄'ün bit set/reset'i ile kontrol edilir.



MODE 2 KONTROL KELİMELERİ

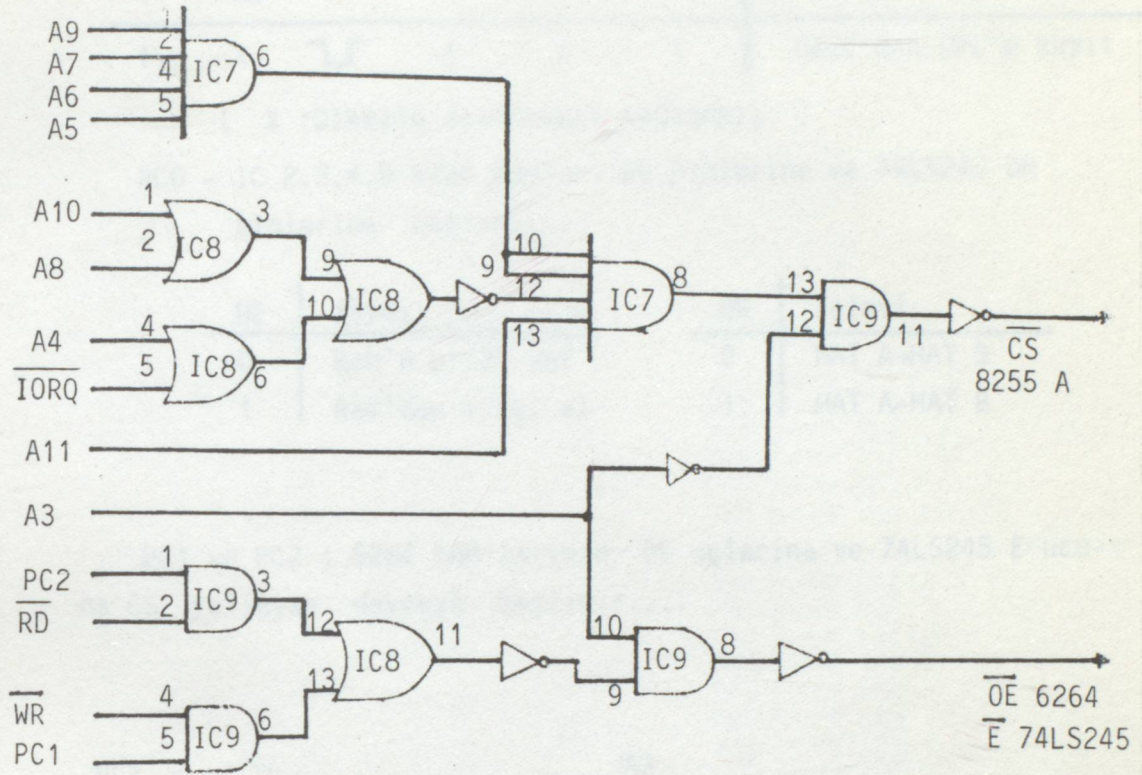


RAM DISC DONANIMI



(RAM Disc blok diyagram)

ADRES ÇÖZÜMLEME DEVRESİ



8255 C Port'unun Ram'lara Chip select üretiminde kullanımı

HEX	PC7	PC6	PC5	PC4	İŞLEVİ
1	0	0	0	1	RAM 1 Chip select
2	0	0	1	0	RAM 2 Chip select
4	0	1	0	0	RAM 3 Chip select
8	1	0	0	0	RAM 4 Chip select

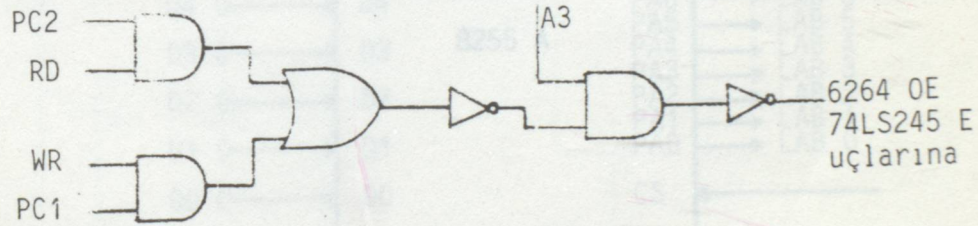
A3	WR	RD	PC2	PC1	PC0	İŞLEV
1		X	0	1	0	CPC'den DISC'e kayıt
1	X		1	0	1	DISC'den CPC'e kayıt

(X :Dikkate alınmaması sağlanmış)

PC0 - IC 2,3,4,5 6264 Ramları WE pinlerine ve 74LS245 DR pinlerine bağlıdır..

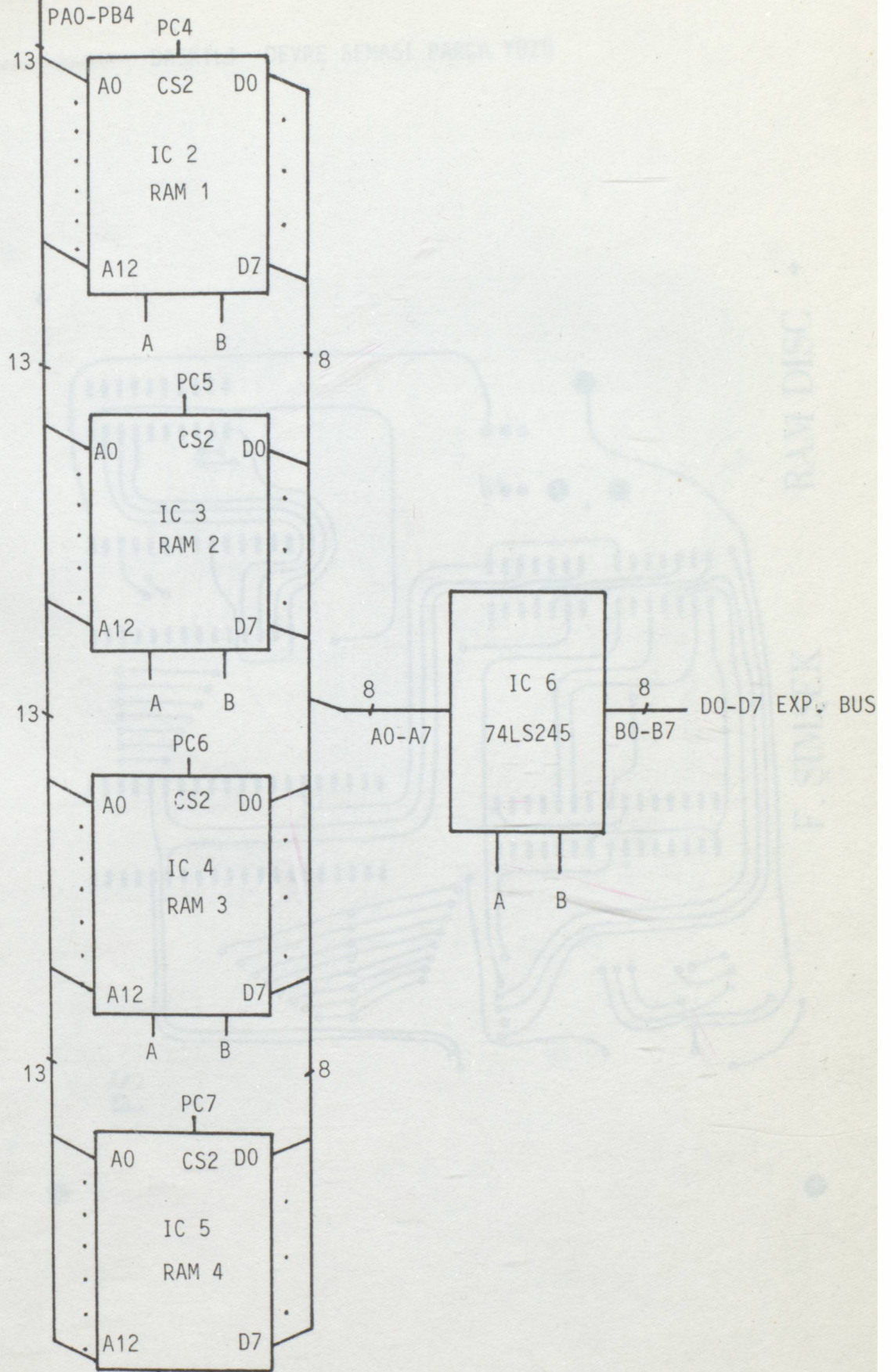
WE	İşlevi	DR	İşlevi
0	Ram'a bilgi yaz	0	HAT A→HAT B
1	Ram'dan bilgi al	1	HAT A←HAT B

PC1 ve PC2 ; 6264 RAM'larının OE uçlarına ve 74LS245 E ucuna CS yollayan devreye bağlıdır....



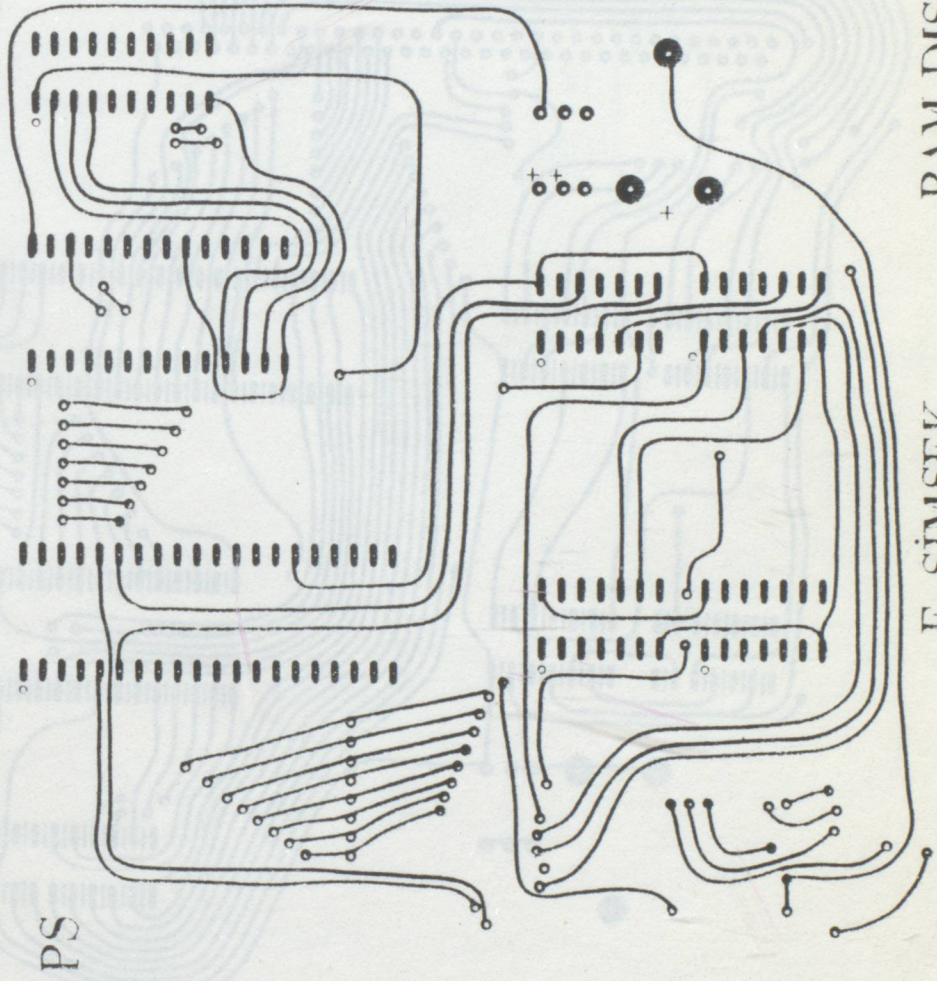
OE ve E işaretlerini üreten yukarıdaki devrede ,8255 A PPI chip'in C portunun, PC1 ve PC2 bitlerinin SET , RESET edilmesi ile disc'den hafızaya kayıt sırasında RD'nin , hafızadan disc'e kayıt sırasında WR' ın aktif olmasını sağlar..

BÖLGESEL ADRES
HATTI



B: ADRES ÇÖZÜMLEME DEVRESİNDEN
A: 8255 PPI CHIP PC0 UCUNDAN . . .

BASKILI DEVRE ŞEMASI PARÇA YÜZÜ

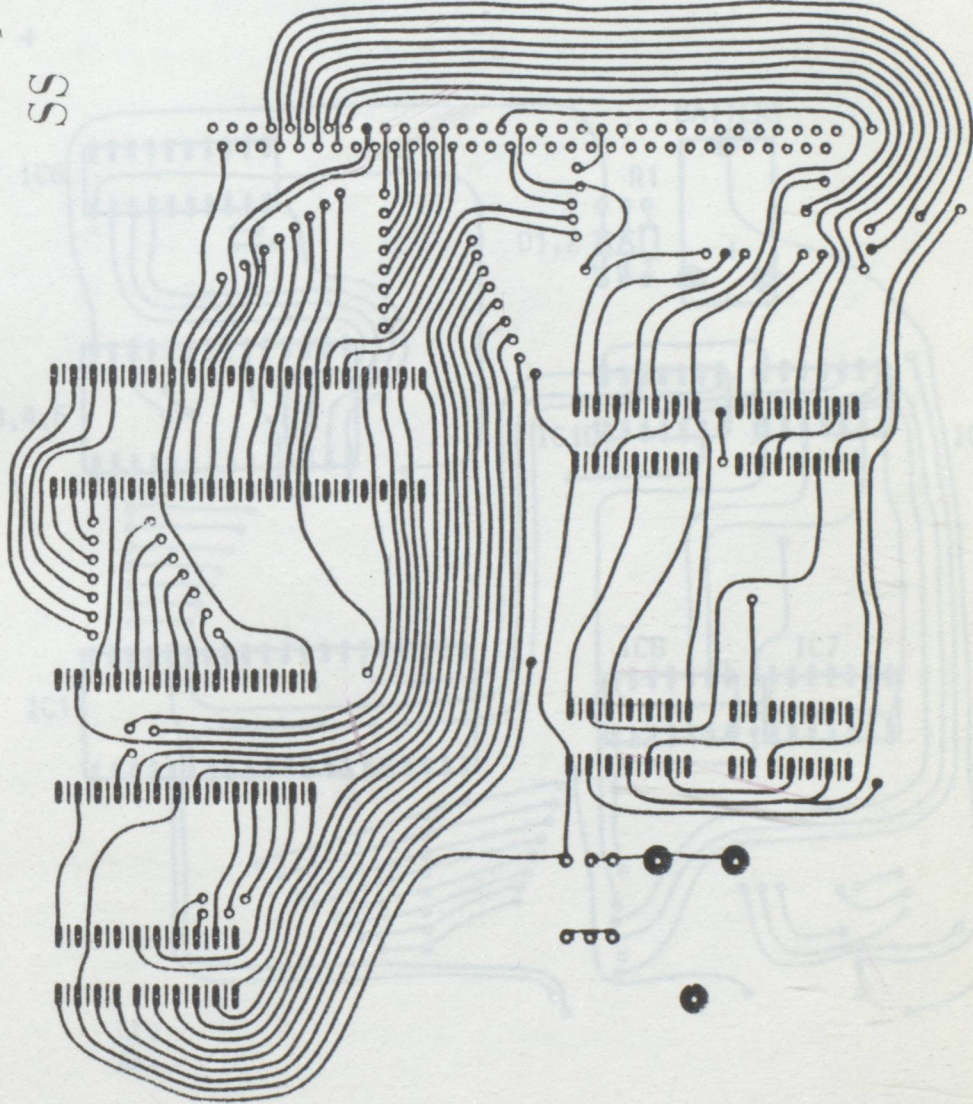


RAM DISC

F. ŞİMŞEK

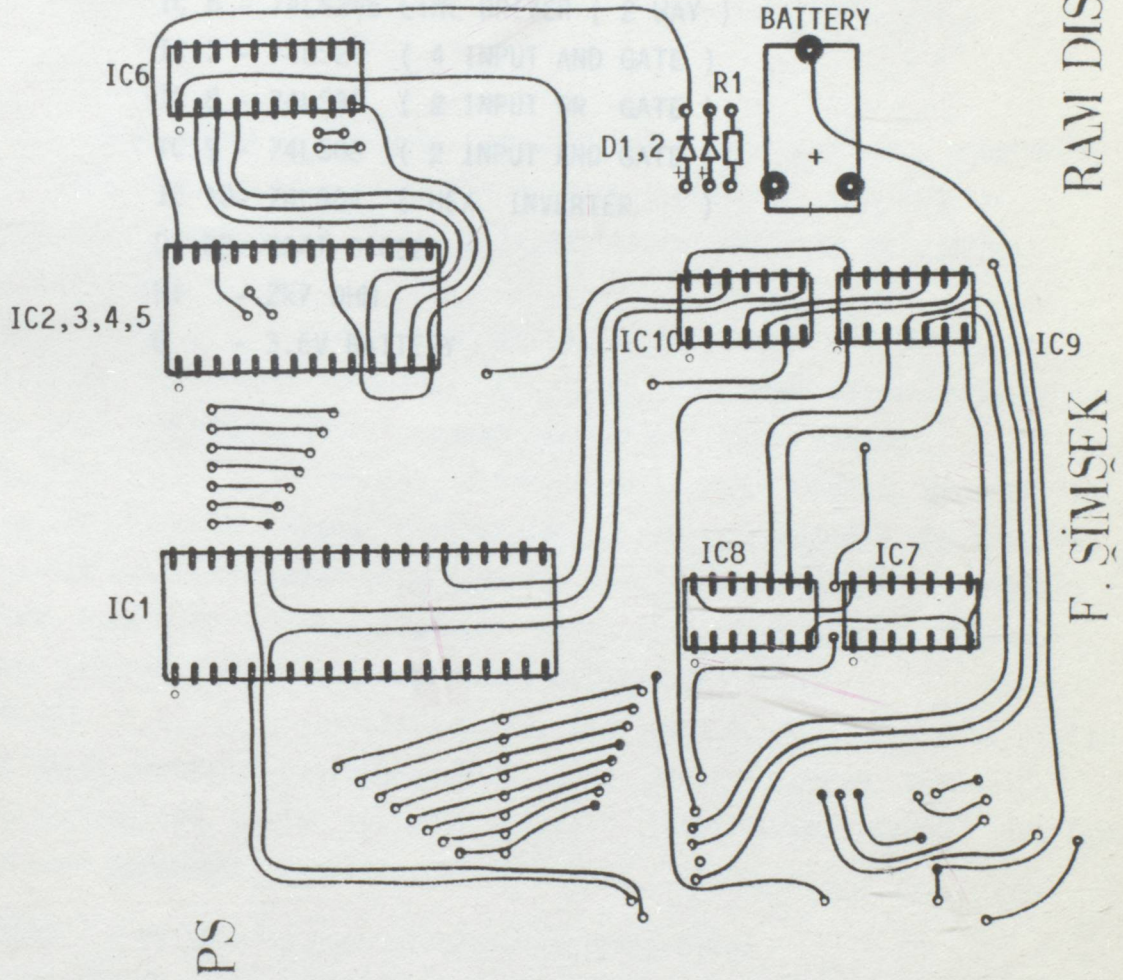
PS

BASKILI DEVRE ŞEMASI LEHİM YÜZÜ



MAİZEME YERLEŞTİRME PLANI

ÜSTTEN GÖRÜNÜŞ



RAM DISC YAZILIMI

PARÇA LİSTESİ

DISC E KAYIT .D

MEMORY/E IC 1 - 8255 A PPI CHIP

PMS. LİST IC 2 - 6264LP RAM CHIP

PMS. SİL IC 3 - 6264LP RAM CHIP

CİKİS IC 4 - 6264LP RAM CHIP

(B/M/L/S/K) IC 5 - 6264LP RAM CHIP

IC 6 - 74LS245 LINE DRIVER (2 WAY)

IC 7 - 74LS21 (4 INPUT AND GATE)

IC 8 - 74LS32 (2 INPUT OR GATE)

IC 9 - 74LS08 (2 INPUT AND GATE)

IC 10- 74LS04 (HEX INVERTER)

D1,D2- 0A47 DIODE

R1 - 2k7 OHM

B - 3.6V BATTERY

RAM DISC YAZILIMI

Program yürütüldüğünde ekranda;

DISC'E KAYIT..D

MEMORY'E KAYIT...M

PRG. LISTESI....L

PRG. SILME.....S

CIKISC

(D/M/L/S/C)

;mesajı görülür.

"D" DISC'E KAYIT

Ana menüde D tusuna basıldığında , ekrana ; basic programların daha önceden yüklendiği RAM no'ları listelenir. Bos RAM'lar , RAM X BOS ;mesajı ile belirlenir.Ram'ların hepsinin dolu olması ihtimali ile ekrana ;

DEVAM ..E/H .. ;kontrolü gelir.Ram'lar dolu ise "H" tusuna basılarak Ana menüye dönülür. "E" tşuna basılarak devam edildiğinde boş olan bir Ram'a Basic program kaydetmek için ekrana;

PRG. ISMI : ;mesajı çıkar.kullanıcının verdiği program ismi karakter karakter ekrana basılır.İsmin yanlış yazılması halinde DEL tuşu ile çıkılıp, tekrar isim verilir.İsim yazma işlemi bittiginde ENTER tuşu ile çıkılıp,programa devam edilir.Ardından ekrana Basic programın kaydedileceği Ram'ı belirlemek için;

RAM NO : ;mesajı çıkar. Klavyeden 1, 2, 3 veya 4 sayılarından biri girilerek,belirlenen Ram içine Basic program yüklenir.

Kayıt sırasında Ram'a yüklenen bilgiler local &0000 - &2000 adresleri arasında aşağıdaki gibidir.

& 0000 - & 25 ;Ram'ın dolu olduğunu gösteren bilgi

& 0001 - & XX ;İsim uzunluk Byte'ı

& 0002 - & XX ;İsmin ilk Hex karakteri

:

n - & XX ;İsmin ilk Hex karakteri

n+1 - & XX ;10 Byte, Basic &AE81 - & AE8A adresleri arasındaki Basic

:

;program başlangıç - bitiş vb. bilgileri saklayan adres

n+11 - & XX ;bilgilerinin transfer edildiği bölge.

n+12 - & XX ;Transfer edilen Basic program

:

& 2000 - & XX ;Basic sonu

Kayıt işlemi bittiğinde ekrana ;
KAYIT SON ; mesajı çıkar.Ardından Ana menü'ye dönülür.

"M" MEMORY'E KAYIT

Disc'de bulunan Basic programlardan herhangi birini Basic bölgesine transfer için, "M" tuşuna basıldığında,ekrana ,sırasıyla 1 2, 3 ve 4 no'lu Ram'lardaki programlar ;

RAM X ABCD formunda,program isimleri belirtilerek ekrana çıkar.Eğer kontrolde Ram'a Basic program yüklenmediği belirlenirse,ekrana ilgili Ram için ;

RAM X BOS ; mesajı gözüktür.Dolu Ram'lardan birinden transfer edilmek istenen Basic programa ait Ram no'su ekrana çıkacak;

RAM NO : ;mesajının ardından, klavyeden verilir.Verilen Ram no'suna göre, ilgili Ram'a PPI chip tarafından uygun Chip select verilerek Ram içindeki bilgilerin alınabilmesi için Ram aktif edilir.Disc deki program ismi geçilip, &AE81 - &AE8A adresleri arasına yüklenmesi gereken 10 Byte'lık Basic başlangıç - bitiş adres bilgileri ,ardından Basic programın kendisi &016F adresinden başlayarak yerleştirilir. Transfer işlemi bittikten sonra ekrana ;

KAYIT SON ; mesajı çıkar ve Ana menü'ye dönülür.

"L" PROGRAM LİSTELEME

Disc'de bulunan Basic programların isimlerini ve hangi Ram'da bulunduklarını listeler. Sırasıyla 1, 2, 3 ve 4 no'lu Ram'lardaki programlar;

RAM X ABCD ;formunda ekrana çıkar.Boş olan Ram varsa ekrana ilgili Ram için;

RAM X BOS ;mesajı çıkar.Örnek olarak,herhangi bir list ekranda,

RAM 1 SPEED1

RAM 2 BOS

RAM 3 BOS

RAM 4 MATCH ,şeklinde olacaktır.

"S" PROGRAM SILME

Ekran formu, program listelemeye olduğu gibi, dolu Ram-lar program isimleriyle, boş Ram'lar boş olduğu belirtilerek düzenlenmiştir. Ardından ekrana silinecek Ram'la ilgili ;

RAM NO : ; mesajıyla klavyeden verilen cevap ile ilgili Ram-daki program silinir. Silme işlemi ilgili Ram'daki &0000 adresinde-ki &25 bilgisi yerine &FF yazılarak yapılır. Silme işlemi bittiğinde Ana menü'ye dönlür.

"C" ÇIKIŞ

Ana menü'de "C" tuşuna basılarak, programdan Assambler programına dönüş sağlanır. Burada "B" tuşuna basarak Basic'e geçip kaydedilen Basic programla çalışılabilir.

R A M D I S C PROGRAM LİSTESİ

; RAM DISC SOFTWARE

```
LD A,&02
CALL &BC0E      ;Mode 2
LD B,&04
CALL SAAT       ;4 satır atlat
MENU:LD B,&71
LD HL,&6100
CALL MESAJ      ;Menüyü Listele
SESA:CALL &BB18  ;Klavye tara
CP & 44         ;D tuşu
JP Z,SAV        ;Disc'e kayıt prg.
CP & 4D         ;M tuşu
JP Z,LOD        ;Memory'e kayıt prg.
CP & 4C         ;L tuşu
JP Z,LIS        ;List etme prg.
CP & 53         ;S tuşu
JP Z,SIL        ;Silme prg.
CP & 43         ;C tuşu
JP Z,CIK        ;Assambler prg.'na dallan
```


;DISC'E YUKLEME PRG.

SAV:CALL &BB5A

LD B,&03

CALL SAAT ;Ekranda 3 satır atla

CALL SART ;PPI Şartla

LD D,& 1A ;Ram 1 Chip select

CALL PRIS

JP Z,RBFL ;RAM 1 DOLU yaz

CALL RAMBB ;RAM 1 BOS yaz

ASSB:LD D,& 2A ;Ram 2 Chip select

CALL PRIS

JP Z,RIFL ;RAM 2 DOLU yaz

CALL RAMBI ;RAM 2 BOS yaz

ASSI:LD D,& 4A ;RAM 3 Chip select

CALL PRIS

JP Z,RUFL ;RAM 3 BOS yaz

CALL RAMBU ;RAM 3 BOS yaz

ASSU:LD D,& 8A ;Ram 4 Chip select

CALL PRIS

JP Z,RDFL ;RAM 4 DOLU yaz

CALL RAMBD ;RAM 4 BOŞ yaz

JP DİGER ;Devam

RBFL:CALL RAM

LD A,& 31

CALL &BB5A

LD A,& 20

CALL &BB5A

CALL FULL

JP ASSB ;Ram 2'yi kontrole git

RIFL:CALL RAM

LD A,& 32

CALL &BB5A

LD A,& 20

CALL &BB5A

CALL FULL

JP ASSI ;Ram 3'ü kontrole git

RUFL:CALL RAM

LD A,& 33

CALL &BB5A

LD A,& 20

CALL &BB5A

CALL FULL

JP ASSU

;Ram 4'ü kontrole git

RDFL:CALL RAM

LD A,& 34

CALL &BB5A

LD A,& 20

CALL &BB5A

CALL FULL

DIGER:LD B,& 0D

LD HL,&6199

CALL MESAJ

;Ekran DEVM..(E/H).. yazıldı

ESIT:CALL &BB18

;Klavye tara

CP & 45

;Evet için E tuşu

JP Z,ETI

;Program ismi iste

CP & 48

;Hayır için H tuşu

JP Z,MENU

;Tüm Ramlar dolu

JP ESIT

ETI:LD B,& 09

LD HL,&617F

CALL MESAJ

;Ekran PRG.ISMI yazdırıldı.

LD HL,&3500

LD B,& 00

TEK:CALL&BB18

;Klavye tara

CP & 0D

;ENTER'e basıldığıнын kontrolü

JP Z,SAS

CALL &BB5A

CP & 7F

;DEL'e basıldığıнын kontrolü

JP Z,DIGER

INC HL

LD (HL),A

;İsim karakterinin ASCII'ni sakla

INC HL

JP TEK

SAS:LD HL,&3500

LD (HL),B

LD HL,&4000

LD (HL),& 25

INC HL

LD DE,&3500

LD A,(DE)

LD (HL),A

INC HL

LD B,A

INC DE

EKSI:LD A,(DE)

LD (HL),A

INC DE

INC HL

DJNZ EKSI

LD DE,&AE81

LD B,& 0A

AKSE:LD A,(DE)

LD (HL),A

INC DE

INC HL

DJNZ AKSE

LD E,L

LD D,H

LD HL,&016F

LD BC,&1FFF

LDIR

LD BC,&FAE3

LD A,& 80

OUT(C),A

LD B,& 01

CALL SAAT

;İsim uzunluğu &3500 'de

;Geçici bellek başı

;Ram'ın dolu olduğunu gösterir bilgi

;İsmin yazıldığı geçici bölge

;4001'deuzunluk var

;B=0 iken isim ve uzunluğu yüklendi

;B=0 iken Basic transferi bitti

;Ekranı 3sattır atlandı.


```

LD B,& 07
LD HL,&6188
CALL MESAJ           ;Ekрана RAM NO: yazıldı
CALL EKA
LD HL,&4000           ;Hazır bilgi bölge başı
EXX
LD HL,&0000           ;Local address bus başlangıcı
ROSE:CALL ERSA
INC HL
LD A,& 20
CP H
JP Z,MESS
JP ROSE
MESS:LD B,& 0A
LD HL,&618F
CALL MESAJ           ;Ekрана KAYIT SON yazıldı
LD B,& 02
CALL SAAT
CALL MENU            ;Kayıt bitti Ana menü'ye dön

;MEMORY'E YUKLEME PRG.

LOD:CALL &BB5A
LD B,& 03
CALL SAAT            ;3 satır atlat
CALL ELIS            ;Ram'ları DOLU ve BOS olarak listele
LD B,& 07
LD HL,&6188
CALL MESAJ           ;Ekрана RAM NO: yazdır
CALL EKA             ;Uygun Ram'a Chip select verildi
CALL COULD
EXX
LD HL,&AE81
EXX
CALL BAND            ;Basic bilgileri yerleşti
CALL DUST            ;Basic prg. transfer edildi
LD B,& 01
CALL SAAT

```



```

LD B,& 0A
LD HL,& 618F
CALL MESAJ ;Ekрана PRG.SONU yazdırıldı
CALL MENU

```

```

;PROGRAM SILME

```

```

SIL:LD B,& 03
CALL SAAT
CALL ELIS ;Ram'ları DOLU ve BOS olarak listele
LD B,& 07
LD HL,&6188
CALL MESAJ ;Ekрана RAM NO: yazıldı
CALL EKA ;Uygun Ram'a chip select verildi
LD HL,&0000
LD BC,&FAE0
OUT(C),L
LD BC,&FAE1
OUT(C),H
LD A,& FF ;Ram'ın &0000'deki &25 yerine &FF yaz
LD BC,&FAE8
OUT(C),A ;&0000'ne &FF yerleştirdi
CALL MENU

```

```

;PROGRAM LİSTELEME

```

```

LIS:LD B,& 03
CALL SAAT
CALL ELIS
CALL MENU

```

```

;ÇIKIŞ PROGRAMI

```

```

CIK:LD B,&02
CALL SAAT
RET ;Assambler prg.'na dönüş

```


ALT PROGRAMLAR

SAV, LOD, SIL, LIS ve CIK programları aşağıdaki altprogramları kullanırlar....Altprogram isimleri;ERSA ,SART ,COUNT ,MESAJ, RAM , FULL ,SAAT ,RAMBB ,RAMBI ,RAMBU ,RAMBD ,PRIS ,ELIS ,COULD ,BAND ,DUST, ve EKA 'dır. Altprogramların bitişinde " * " işareti programların gözle ayırılabilmesi için kullanılmıştır..

;SUBROUTINES

EKA:CALL &BB18 ;Klavyeden girilen sayı ile Ram'a CS üret.

CP &31

JP Z,BIR

CP &32

JP Z,IKI

CP &33

JP Z,UC

CP &34

JP Z,DORT

JP EKA

BIR:CALL &BB5A

LD D, &1A

;RAM 1 CS

LD BC ,&FAE2

OUT(C),D

JP ETSE

IKI:CALL &BB5A

LD D, &2A

RAM 2 CS

LD BC ,&FAE2

OUT(C),D

JP ETSE

UC:CALL &BB5A

LD D, &4A

;RAM 3 CS

LD BC ,&FAE2

OUT(C),D

JP ETSE

DORT:CALL &BB5A

LD D ,&8A

;RAM 4 CS

LD BC ,&FAE2

OUT(C),D

ETSE:RET

;*****

;Ram dolu ise prg.ismini,boş ise RAM BOS yazdırma

ELIS:CALL SART

LD D ,&1A ;Ram 1 CS

CALL BAY

JP Z,RBIS

CALL RAMBB

RID:LD D ,&2A ;Ram 2 CS

CALL BAY

JP Z,RIIS

CALL RAMBI

RUD:LD D ,&4A ;Ram 3 CS

CALL BAY

JP Z,RUIS

CALL RAMBU

RDF:LD D ,&8A ;Ram 4. CS

CALL BAY

JP Z,RDIS

CALL RAMBD

RAF:RET

BAY:LD BC ,&FAE2

OUT(C),D

LD HL ,&0000

CALL COUNT

CP &25

RET

RBIS:CALL RAM

LD A ,&31

CALL IKS

JP RID

RIIS:CALL RAM

LD A ,&32

CALL IKS

JP RUD

RUIS:CALL RAM

LD A ,&33

CALL IKS

JP RDF

RDIS:CALL RAM

LD A ,&34

CALL IKS

JP RAF

IKS:CALL &BB5A

LD A ,&20

CALL &3B5A

LD HL,&0001

CALL COUNT

LD B ,A

EMA:INC HL

CALL COUNT

CALL &BB5A

DJNZ EMA

RET

;*****

;SAV prg.'da locall address bus saydırma

ERSA:LD BC,&FAE0

OUT(C),L

LD BC,&FAE1

OUT(C),H

EXX

LD A,(HL)

LD BC,&FAE8

OUT(C),A

INC HL

EXX

RET

;*****

;PPI Chip'i OUT olarak şartlandırma

SART:LD BC,&FAE3

LD A,&80

OUT(C),A

RET

;*****

4J

```
        ;B registerine karakter adedi,HL registerine tablo  
        ;başlangıç adresi yükleyerek ekrana mesaj bastırma  
MESAJ:LD A,(HL)  
        CALL &BB5A  
        INC HL  
        DJNZ MESAJ  
        RET  
        ;*****
```

```
COUNT:LD BC,&FAE0  
        OUT(C),L  
        LD BC,&FAE1  
        OUT(C),H  
        LD A,(HL)  
        LD BC,&FAE8  
        OUT(C),A  
        RET  
        ;*****
```

```
        ;B registerine yüklenen sayı kadar satır atlanır  
SAAT:LD A,&0A          ; CR  
        CALL &BB5A  
        LD A,&0D          ; LF  
        CALL &BB5A  
        DJNZ SAAT  
        RET  
        ;*****
```

```
        ;Ekrana RAM yazdırma  
RAM: LD B,&03  
        LD HL,& 6171  
        CALL MESAJ  
        RET  
        ;*****
```

```
        ;Ekrana DOLU yazdırma  
FULL:LD B,&04  
        LD HL,& 6174  
        CALL MESAJ  
        RET  
        ;*****
```



```
        ;Ekrana RAM1 BOS yazma
RAMBB:CALL RAM
        LD A,&31
        CALL EKSAM
        RET
        ;*****

        ;Ekrana RAM2 BOS yazma
RAMBI:CALL RAM
        LD A,&32
        CALL EKSAM
        RET
        ;*****

        ;Ekrana RAM3 BOS yazma
RAMBU:CALL RAM
        LD A,&33
        CALL EKSAM
        RET
        ;*****

        ;Ekrana RAM4 BOS yazma
RAMBD:CALL RAM
        LD A,&34
        CALL EKSAM
        RET
        ;*****

EKSAM:CALL &BB5A
        LD A,&20
        CALL &BB5A
        LD B,&03
        LD HL,& 617A
        CALL MESAJ
        RET
        ;*****
```



```
      ;&0000 adresinin kontrolü  
PRIS:LD BC,&FAE2  
      OUT(C),D  
      LD HL,&0000  
      CALL COUNT  
      CP &25  
      RET  
      ;*****
```

```
COULD:LD HL,&0001  
      LD BC,&FAE0  
      OUT(C),L  
      LD BC,&FAE1  
      OUT(C),H  
      LD BC,&FAE8  
      IN A,(C)  
      LD B,A  
BEER:INC HL  
      DJNZ BEER  
      INC HL  
      RET  
      ;*****
```

```
BAND:LD BC,&FAE0  
      OUT(C),L  
      LD BC,FAE1  
      OUT(C),H  
      EXX  
      LD BC,&FAE8  
      IN A,(C)  
      LD (HL),A  
      LD A,&8A  
      CP L  
      JP Z,MATC  
      INC HL  
      EXX  
      INC HL  
      JP BAND  
MATC:INC HL  
      RET  
      ;*****
```


DUST:LD BC,&FAEO

OUT(C),L

LD BC,&FAE1

OUT(C),H

EXX

LD BC,&FAE8

IN A,(C)

LD (HL),A

LD A,&20

CP H

JP Z,CAMEL

INC HL

EXX

INC HL

JP DUST

CAMEL:INC HL

RET

;*****

EKRANA BASILAN MESAJLAR

Mesajların ekrana çıkarılmasında ; bellekteki boş bir bölgeye yerleştirilen, mesaj bloklarını oluşturan karakterlerin her birinin Hex karşılıklarını alarak ardarda ekrana çıkarma yöntemi kullanılır. Bu tablo &6100 adresinden başlanarak yerleştirilmiştir.

Örnek olarak ;

& 6100 - &50 - P

& 6101 - &52 - R

& 6102 - &47 - G

⋮ ⋮ ⋮

tablosunu kullanarak, ekrana PRG karakterlerini bastırmak için, HL registerine kullanılacak bloğun tablodaki başlangıç adresini, B registerine Byte uzunluğunu yükledikten sonra MESAJ altprogramı çağrılır.

LD B,&03

LD HL,&6100

CALL MESAJ

;programı yürütüldüğünde ekrana PRG

karakterleri çıkar..

Ram Disc yazılımında kullanılan bu tablo yardımıyla aşağıdaki mesajlar ekrana çıkar..

DISC'E KAYIT..D

RAM

MEMORY'E KAYIT..M

DOLU

PRG. SILME....S

BOS

PRG. LISTESI..L

PRG ISMI:

CIKIS.....C

RAM NO:

(D/M/L/S/C).....

KAYIT SONU

DEVAM (E/H):

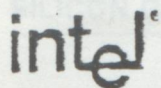
Aşağıda hazırlanmış tablo,ekrana mesaj bastırmak için düzenlenmiştir.

6100 -	44	49	53	43	60	45	20	20	20	4B	41	59	49	54	2E	2E
6110 -	44	0A	0D	4D	45	4D	4F	52	59	60	45	20	4B	41	59	49
6120 -	54	2E	2E	4D	0A	0D	50	52	47	2E	20	20	4C	49	53	54
6130 -	45	53	49	2E	2E	2E	4C	0A	0D	50	52	47	2E	20	20	20
6140 -	20	53	49	4C	4D	45	2E	2E	2E	53	0A	0D	43	49	4B	49
6150 -	53	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	43	0A	0D	0A
6160 -	0D	28	44	2F	4D	2F	4C	2F	53	2F	43	29	2E	2E	2E	2E
6170 -	2E	52	41	4D	44	4F	4C	55	0A	0D	42	4F	53	0A	0D	50
6180 -	52	47	20	49	53	4D	49	3A	52	41	4D	20	4E	4F	3A	4B
6190 -	41	59	49	54	20	53	4F	4E	55	44	45	56	41	4D	20	20
61A0 -	28	45	2F	48	29	3A										

Yukarıdaki tabloda yer alan adres gözlerindeki Hex sayıların,ASCII karşılıkları, aşağıdadır..

6100 -	D	I	S	C	'	E	b	b	b	K	A	Y	I	T	.	.
6110 -	D	CR	LF	M	E	M	O	R	Y	'	E	b	K	A	Y	I
6120 -	T	.	.	M	CR	LF	P	R	G	.	b	b	L	I	S	T
6130 -	E	S	I	.	.	.	L	CR	LF	P	R	G	.	b	b	b
6140 -	b	S	I	L	M	E	.	.	.	S	CR	LF	C	I	K	I
6150 -	S	.	.	.	.	.	.	.	.	.	.	.	C	CR	LF	CR
6160 -	LF	(	D	/	M	/	L	/	S	/	C	)	.	.	.	.
6170 -	.	R	A	M	D	O	L	U	CR	LF	B	O	S	CR	LF	P
6180 -	R	G	b	I	S	M	I	:	R	A	M	b	N	O	:	K
6190 -	A	Y	I	T	b	S	O	N	U	D	E	V	A	M	b	b
61A0 -	(	E	/	H	)	:										

Tabloda gözüken " b " karakteri boşluk belirtir..



Silicon Gate MOS 8255

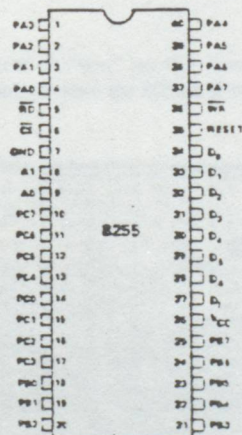
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with MCS™ -8 and MCS™ -80 Microprocessor Families
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual In-Line Package
- Reduces System Package Count

The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bidirectional Bus mode which uses 8 lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

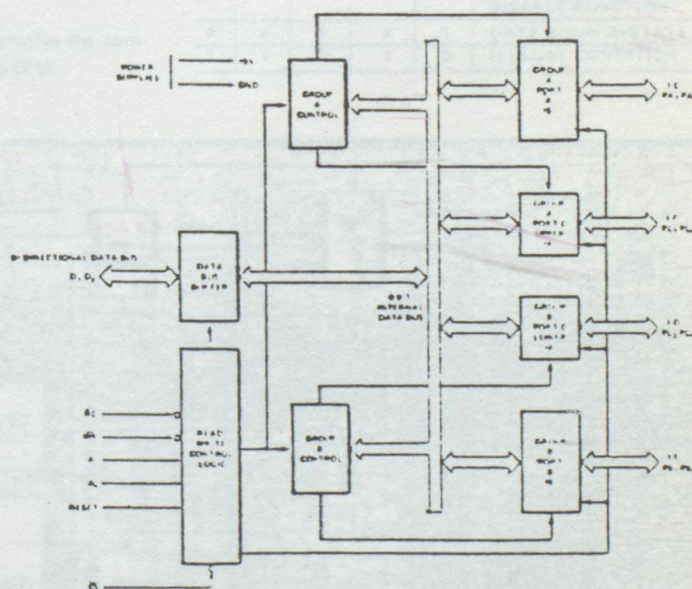
PIN CONFIGURATION



PIN NAMES

D ₀ -D ₁₅	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
AC A1	PORT ADDRESS
PA7-PA2	PORT A (BIT)
PB7-PB2	PORT B (BIT)
PC7-PC2	PORT C (BIT)
VCC	+5 VOLTS
GND	0 VOLTS

8255 BLOCK DIAGRAM



SILICON GATE MOS 8255

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INPUT or OUTPUT instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

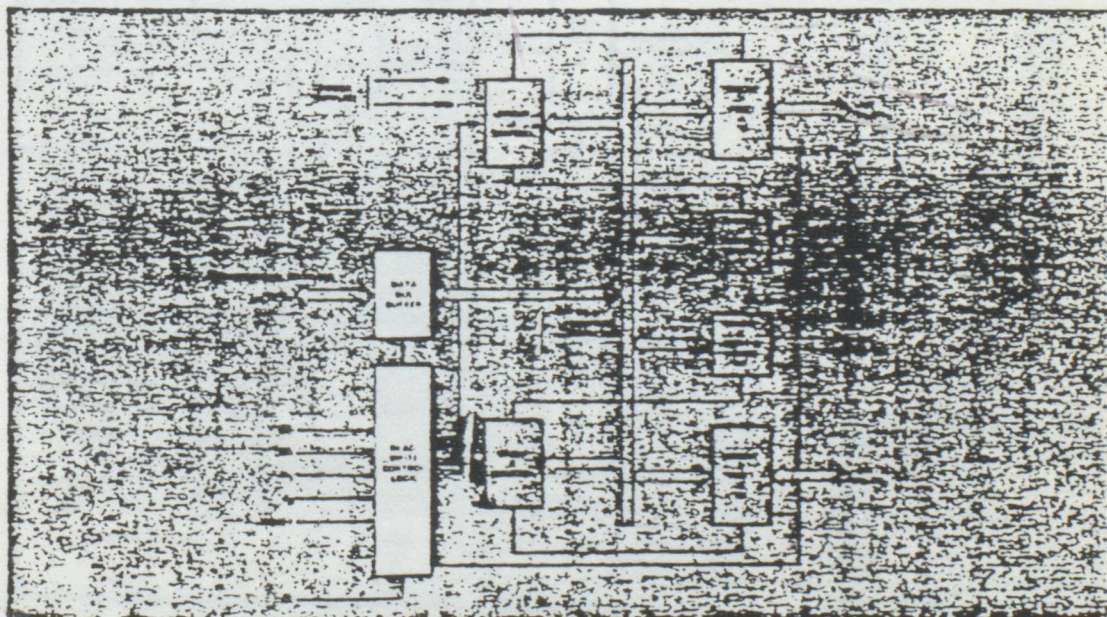
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A = DATA BUS
0	1	0	1	0	PORT E = DATA BUS
1	0	0	1	0	PORT C = DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS = PORT A
0	1	1	0	0	DATA BUS = PORT E
1	0	1	0	0	DATA BUS = PORT C
1	1	1	0	0	DATA BUS = CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS = 3-STATE
1	1	0	1	0	ILLEGAL CONDITION



8255 Block Diagram

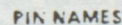
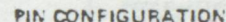
or "prophetic" to further enhance the power and flexi-

Dirty or the EZS.

...and the β value is the slope of the regression line.

bit port contains a 4-bit latch and it can be used for the

Control Group E = Post B and Post C (over 163 GPa)



E ₂	DATABUS BI-DIRECTIONAL
RBS1T	RESET INPUT
E ₂	CMP SELECT
R ₂	READ INPUT
W ₂	WRITE INPUT
AC A1	PORT ADDRESSES
PATPAC	PORT A IS "
PSTPAC	PORT B IS "
PCTPAC	PORT C IS "
VOL	+5 VOLTS
GND	GROUND

SILICON GATE MOS 8255

8255 DETAILED OPERATIONAL DESCRIPTION

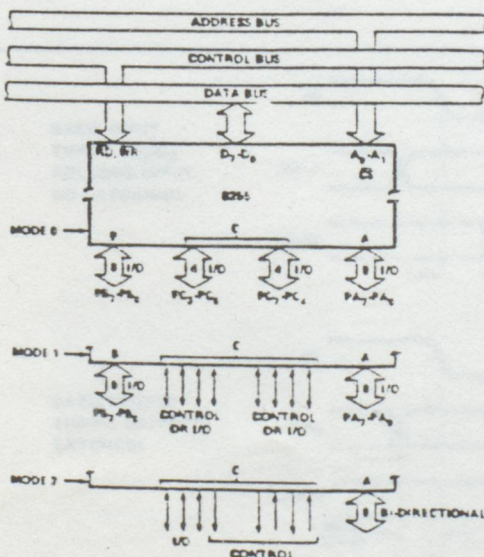
Mode Selection

There are three basic modes of operation that can be selected by the system software:

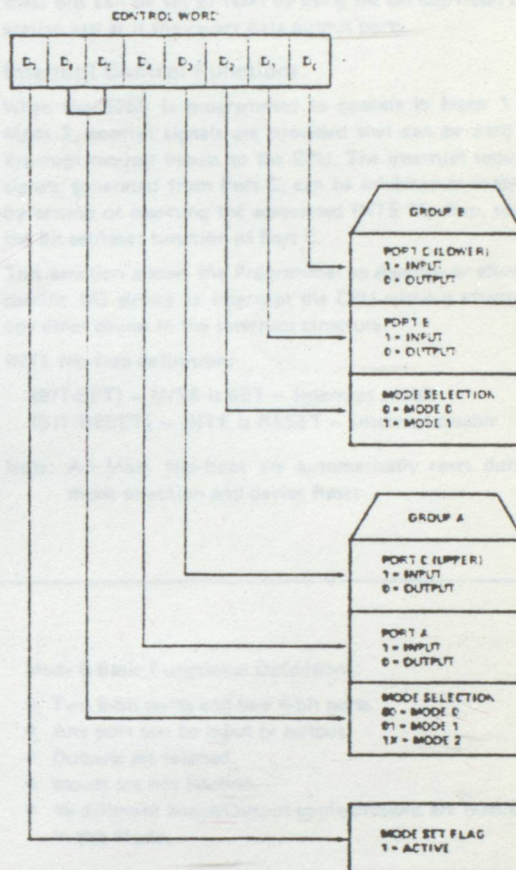
- Mode 0 - Basic Input/Output
- Mode 1 - Strobed Input/Output
- Mode 2 - Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTPUT instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface



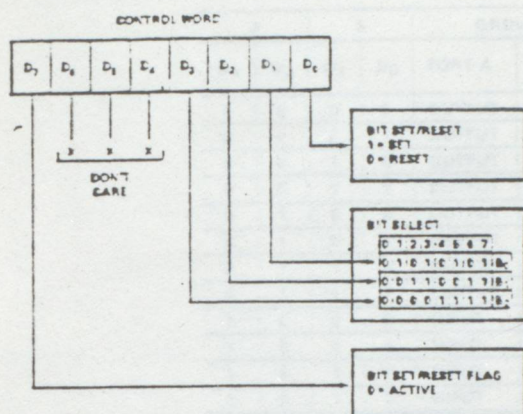
Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTPUT instruction. This feature reduces software requirements in Control-based applications.

SILICON GATE MOS 8255



Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without effecting any other device in the interrupt structure.

INTE flip-flop definition:

- (BIT-SET) – INTE is SET – Interrupt enable
- (BIT-RESET) – INTE is RESET – Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

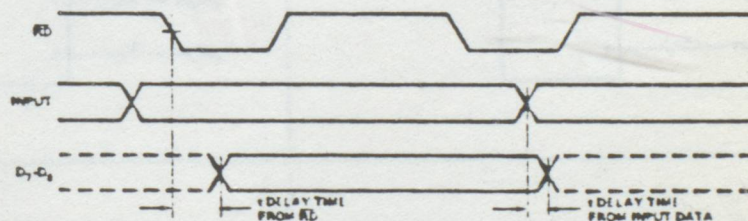
Mode 0 (Basic Input/Output)

This functional configuration provides simple Input and Output operations for each of the three ports. No "hand-shaking" is required, data is simply written to or read from a specified port.

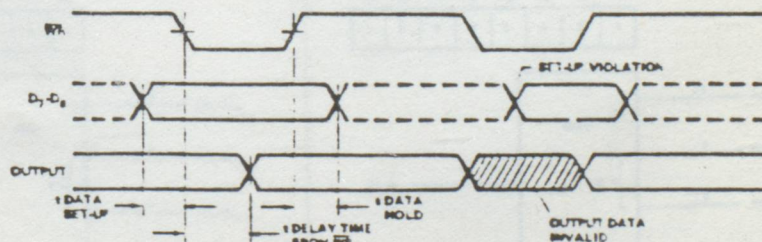
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

**BASIC INPUT
TIMING (D₇-D₀
FOLLOWS INPUT,
NO LATCHING)**



**BASIC OUTPUT
TIMING (OUTPUTS
LATCHED)**



Mode 0 Timing

SILICON GATE MOS 8255

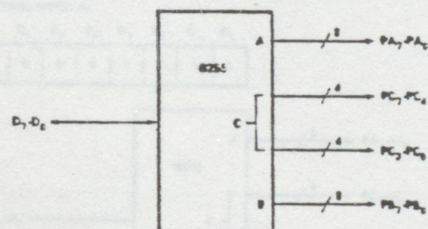
MODE 0 PORT DEFINITION CHART

A		E		GROUP A			GROUP E	
D ₄	D ₃	D ₁	D ₀	PORT A	PORT C (UPPER)	n	PORT E	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 CONFIGURATIONS

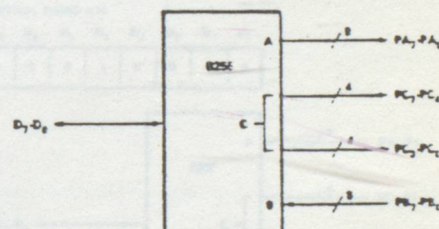
CONTROL WORD #0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	0	0



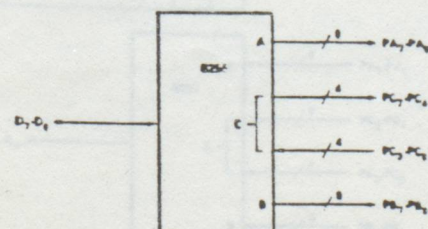
CONTROL WORD #2

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	1	0



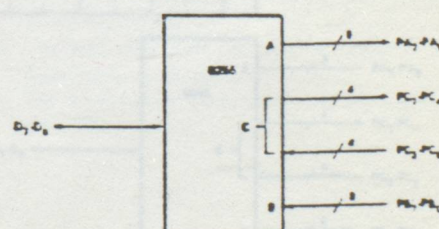
CONTROL WORD #1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	0	1



CONTROL WORD #3

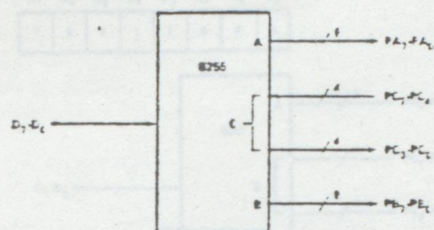
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	0	0	1	1



SILICON GATE MOS 8255

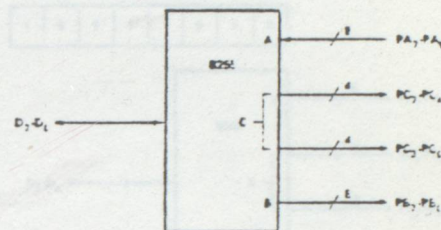
CONTROL WORD #4

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	0	0



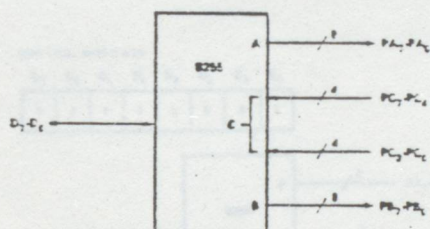
CONTROL WORD #5

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	0	0



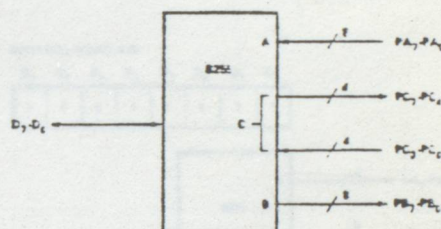
CONTROL WORD #6

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	0	1



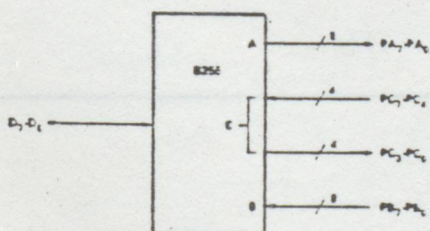
CONTROL WORD #8

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	1	1



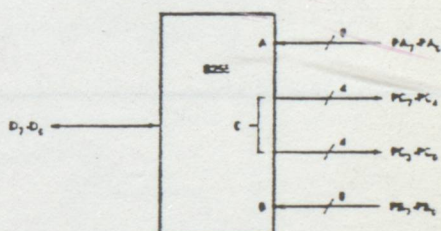
CONTROL WORD #9

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	1	0



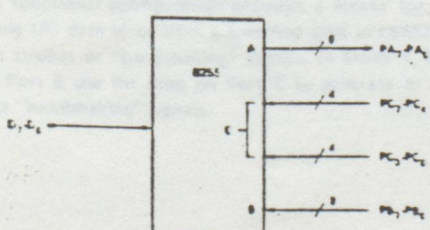
CONTROL WORD #10

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	1	0



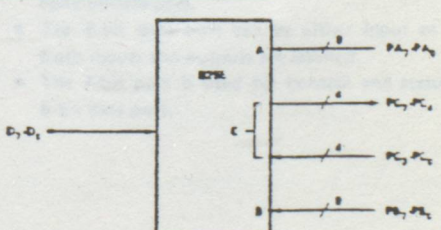
CONTROL WORD #7

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	1	0	1	1

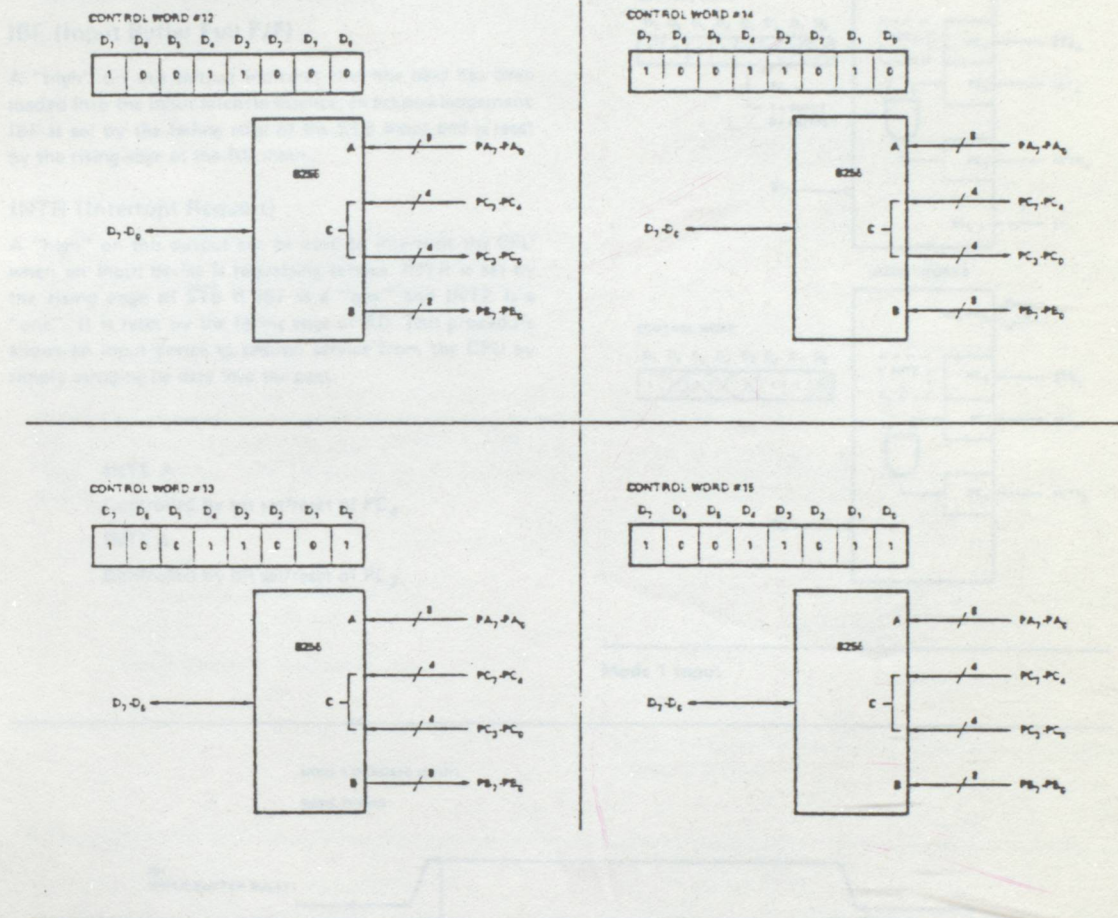


CONTROL WORD #11

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	0	0	1	1



SILICON GATE MOS 8255



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port E use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

SILICON GATE MOS 8255

Input Control Signal Definition

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by the falling edge of the STB input and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

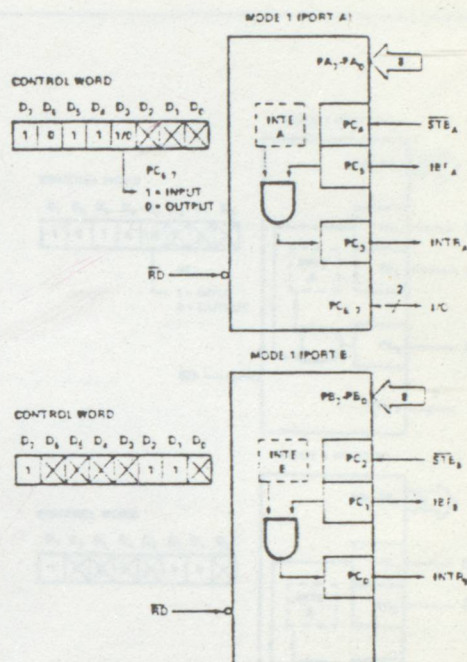
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of STB if IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

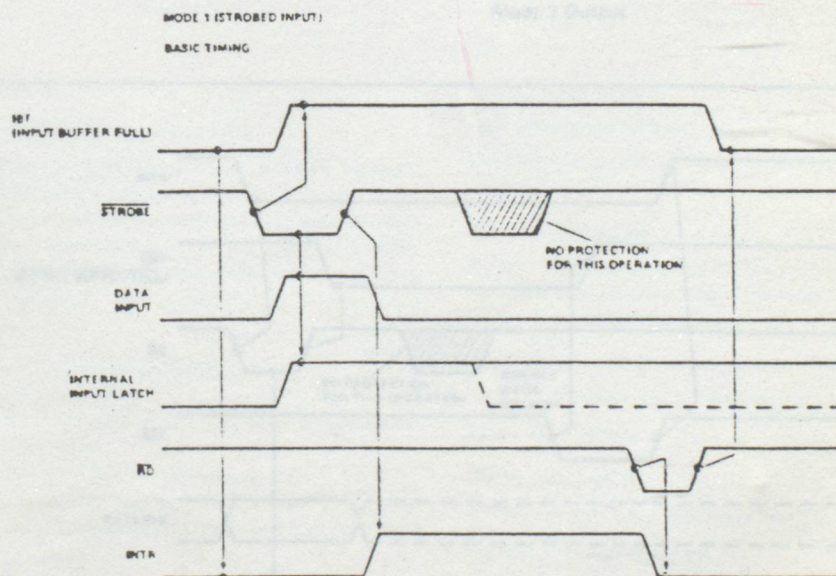
Controlled by bit set/reset of PC₄.

INTE B

Controlled by bit set/reset of PC₂.



Mode 1 Input



Basic Timing Input

SILICON GATE MOS 8255

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by the falling edge of the $\overline{ACK}$ input signal.

$\overline{ACK}$ (Acknowledge Input)

A "low" on this input informs the 8255 that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request)

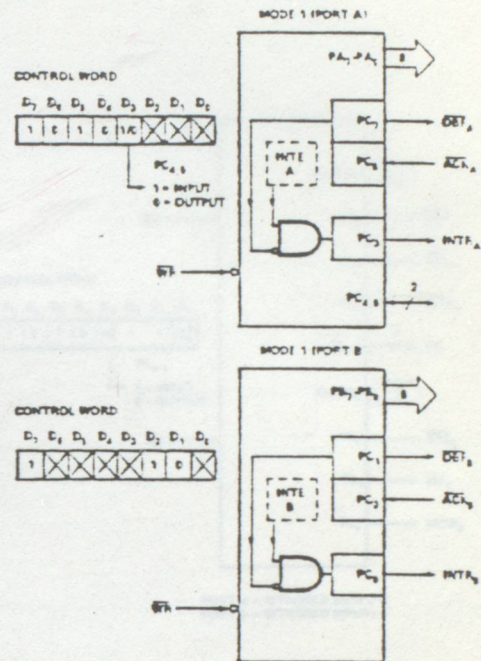
A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of $\overline{ACK}$ if $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

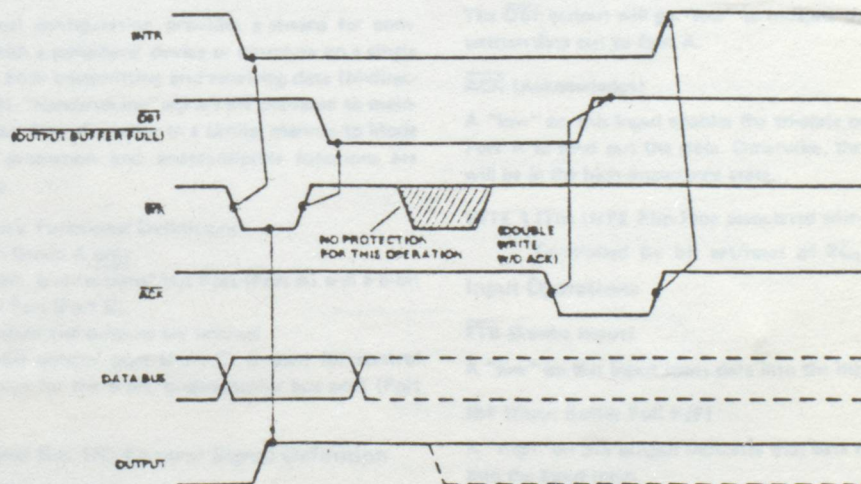
Controlled by bit set/reset of PC_6 .

INTE B

Controlled by bit set/reset of PC_2 .

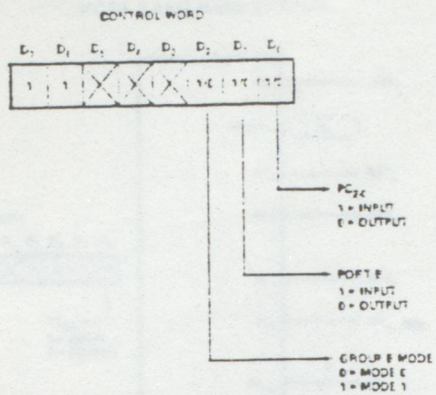


Mode 1 Output

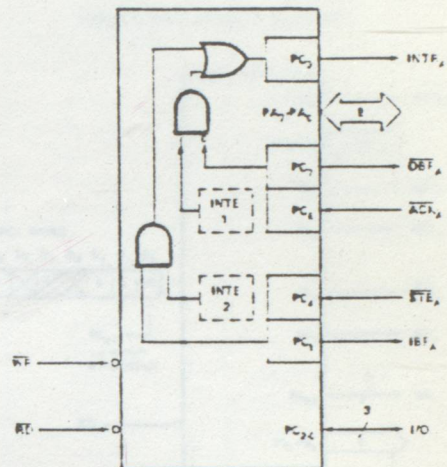


Basic Timing Output

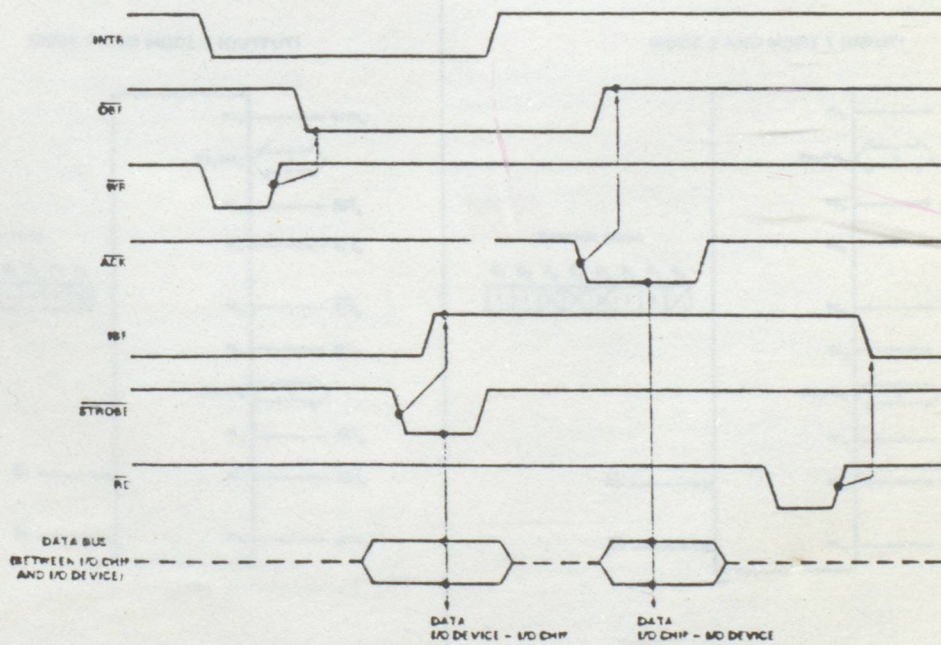
SILICON GATE MOS 8255



Mode 2 Control Word



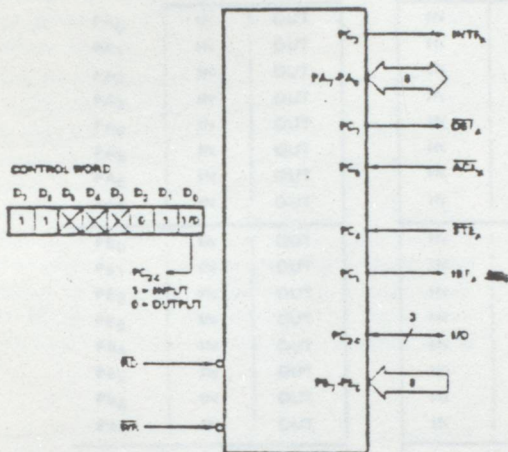
Mode 2



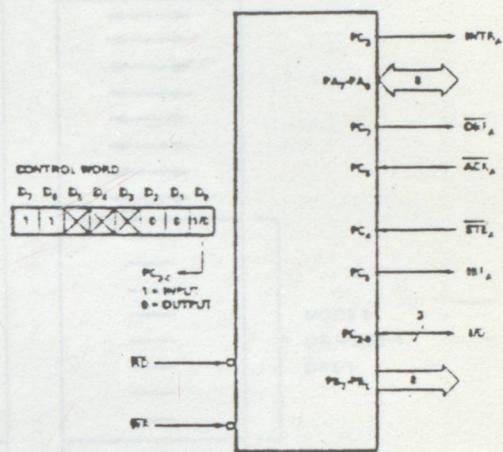
Mode 2 (Bi-directional) Timing

SILICON GATE MOS 8255

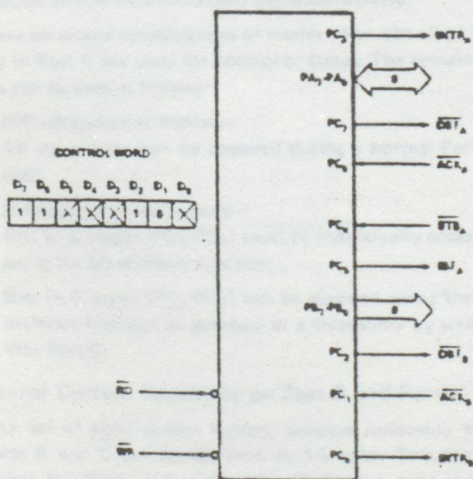
MODE 2 AND MODE 0 (INPUT)



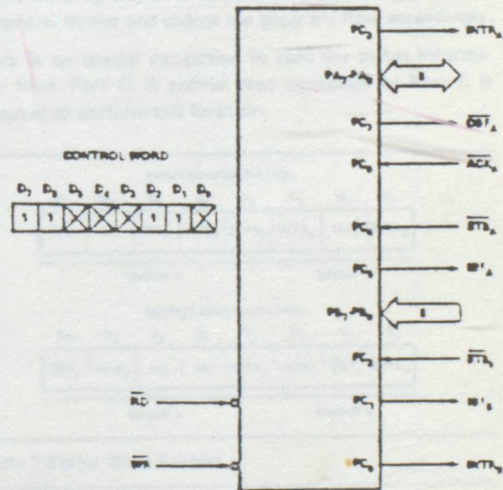
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



MODE DEFINITION SUMMARY TABLE

MODE 0			MODE 1		MODE 2 GROUP A ONLY
	IN	OUT	IN	OUT	
PA ₀	IN	OUT	IN	OUT	
PA ₁	IN	OUT	IN	OUT	
PA ₂	IN	OUT	IN	OUT	
PA ₃	IN	OUT	IN	OUT	
PA ₄	IN	OUT	IN	OUT	
PA ₅	IN	OUT	IN	OUT	
PA ₆	IN	OUT	IN	OUT	
PA ₇	IN	OUT	IN	OUT	
PB ₀	IN	OUT	IN	OUT	
PB ₁	IN	OUT	IN	OUT	
PB ₂	IN	OUT	IN	OUT	
PB ₃	IN	OUT	IN	OUT	
PB ₄	IN	OUT	IN	OUT	
PB ₅	IN	OUT	IN	OUT	
PB ₆	IN	OUT	IN	OUT	
PB ₇	IN	OUT	IN	OUT	
PC ₀	IN	OUT	INTR _B	INTR _B	I/O
PC ₁	IN	OUT	IBF _B	OB _F _B	I/O
PC ₂	IN	OUT	ST _B _B	ACK _B	I/O
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A
PC ₄	IN	OUT	ST _B _A	I/O	ST _B _A
PC ₅	IN	OUT	IBF _A	I/O	IBF _A
PC ₆	IN	OUT	I/O	ACK _A	ACK _A
PC ₇	IN	OUT	I/O	OB _F _A	OB _F _A

MODE 0
OR MODE 1
ONLY

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs —

All input lines can be accessed during a normal Port C read.

If Programmed as Outputs —

Bits in C upper (PC₇-PC₄) must be individually accessed using the bit set/reset function.

Bits in C lower (PC₃-PC₀) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INPUT CONFIGURATION

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
MC	MC	IBF _A	INT _B _A	INT _B _A	INT _B _A	IBF _B	INTR _B

GROUP A

GROUP B

OUTPUT CONFIGURATION

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
OB _F _A	INT _B _A	MC	MC	INT _B _A	INT _B _A	OB _F _B	INTR _B

GROUP A

GROUP B

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C

Mode 1 Status Word Format

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
OB _F _A	INT _B _A	IBF _A	INT _B _A	INT _B _A	INT _B _A	INT _B _A	INT _B _A

GROUP A

GROUP B

DEFINED BY MODE 0 OR MODE 1 SELECTION

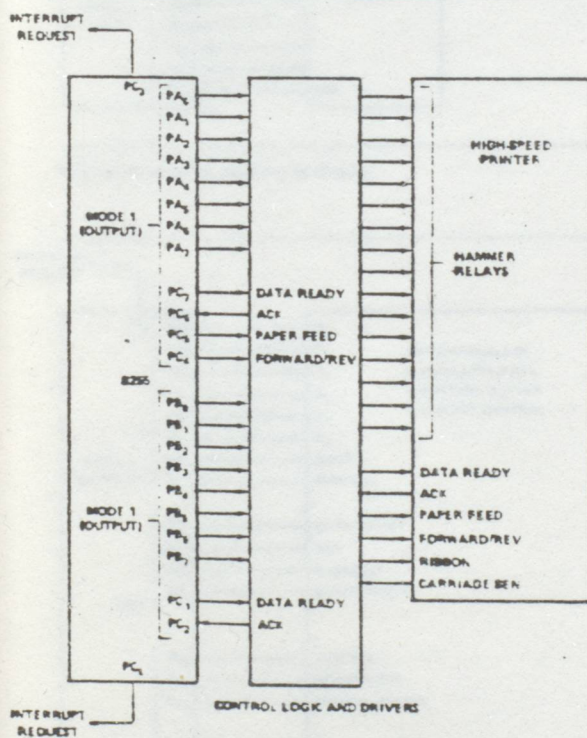
Mode 2 Status Word Format

SILICON GATE MOS 8255

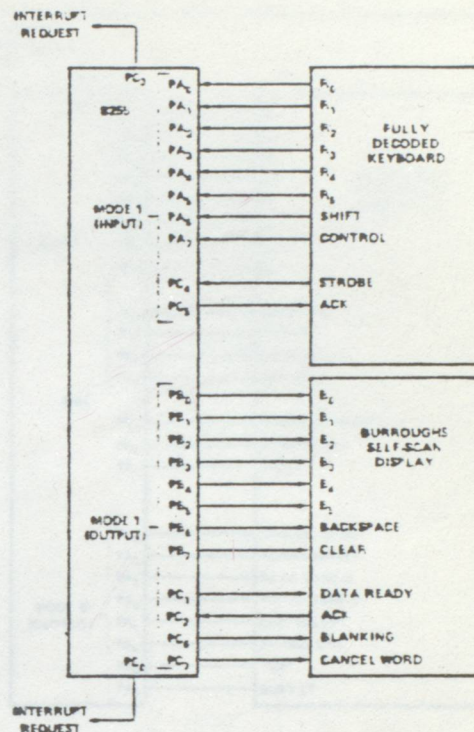
APPLICATIONS OF THE 8255

The 8255 is a very powerful tool for interfacing peripheral equipment to the 8080 microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

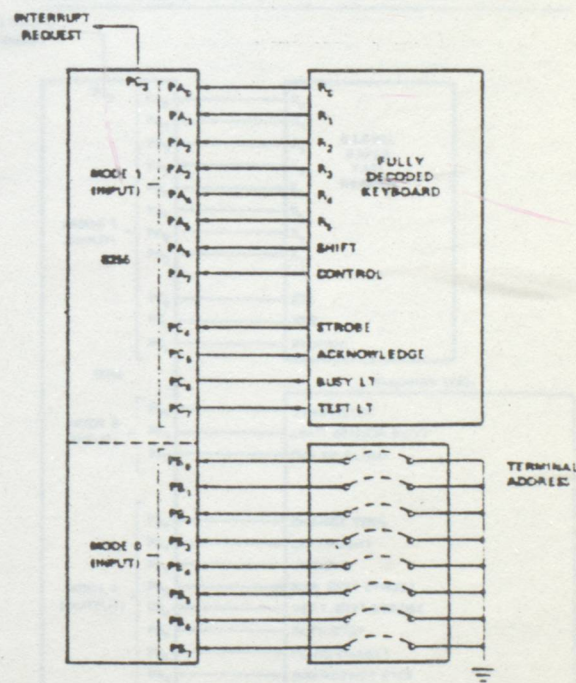
Each peripheral device in a Microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255 is programmed by the I/O service routine and becomes an extension of the systems software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the Detailed Operational Description, a control word can easily be developed to initialize the 8255 to exactly "fit" the application. Here are a few examples of typical applications of the 8255.



Printer Interface

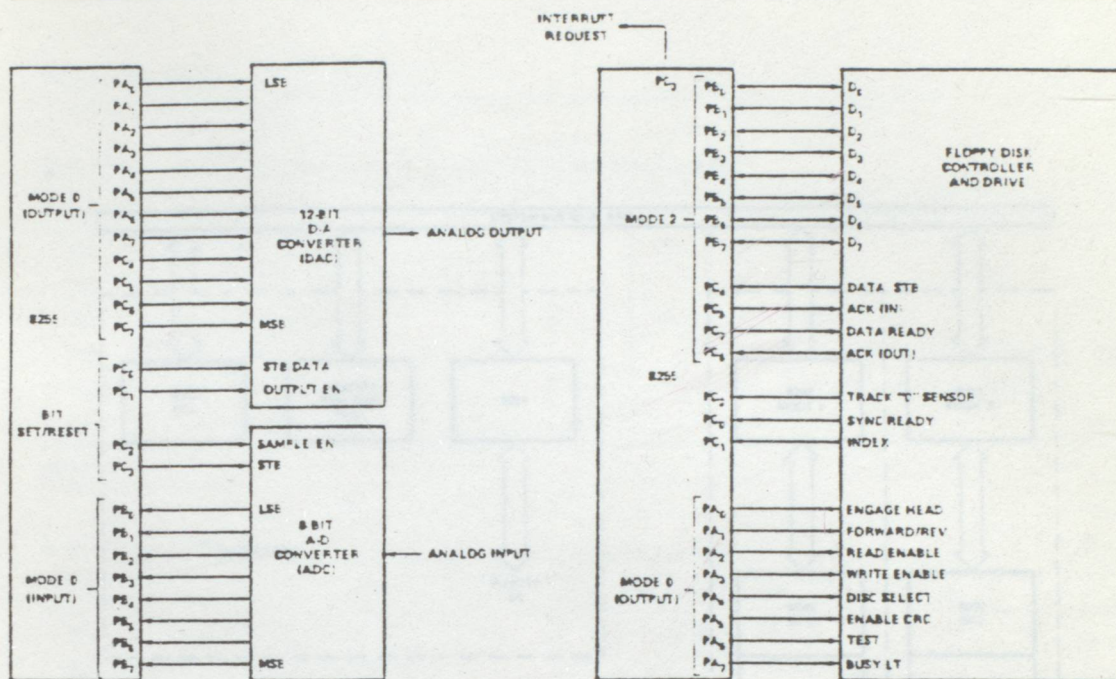


Keyboard and Display Interface



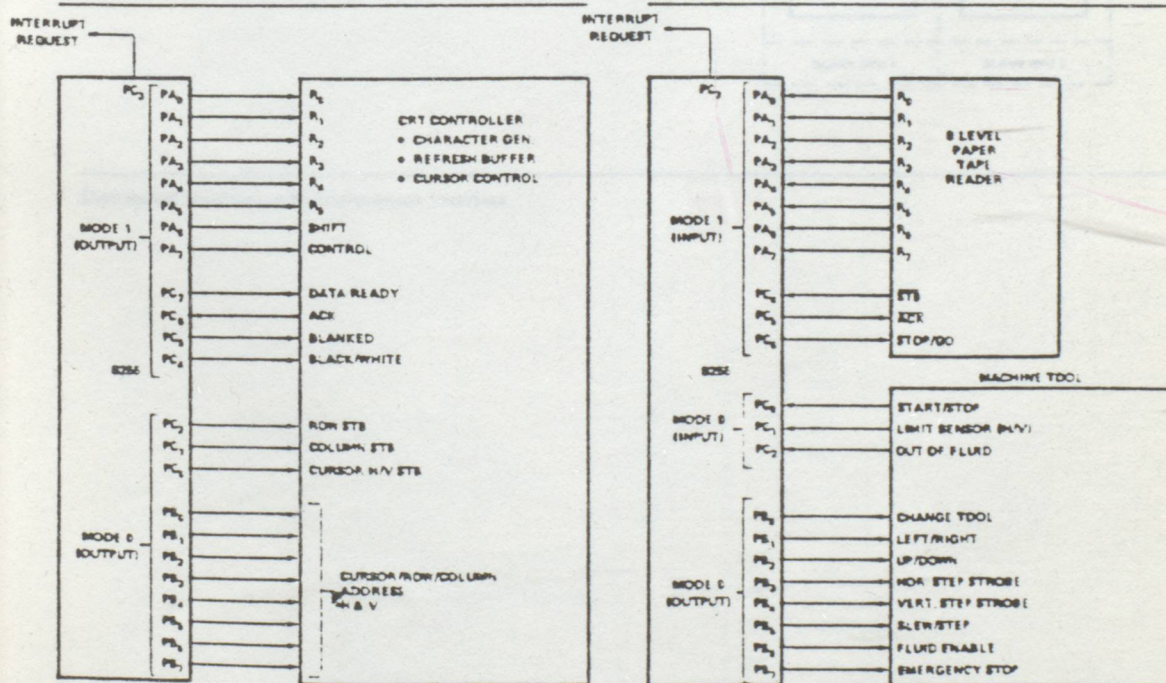
Keyboard and Terminal Address Interface

SILICON GATE MOS 8255



Digital to Analog, Analog to Digital

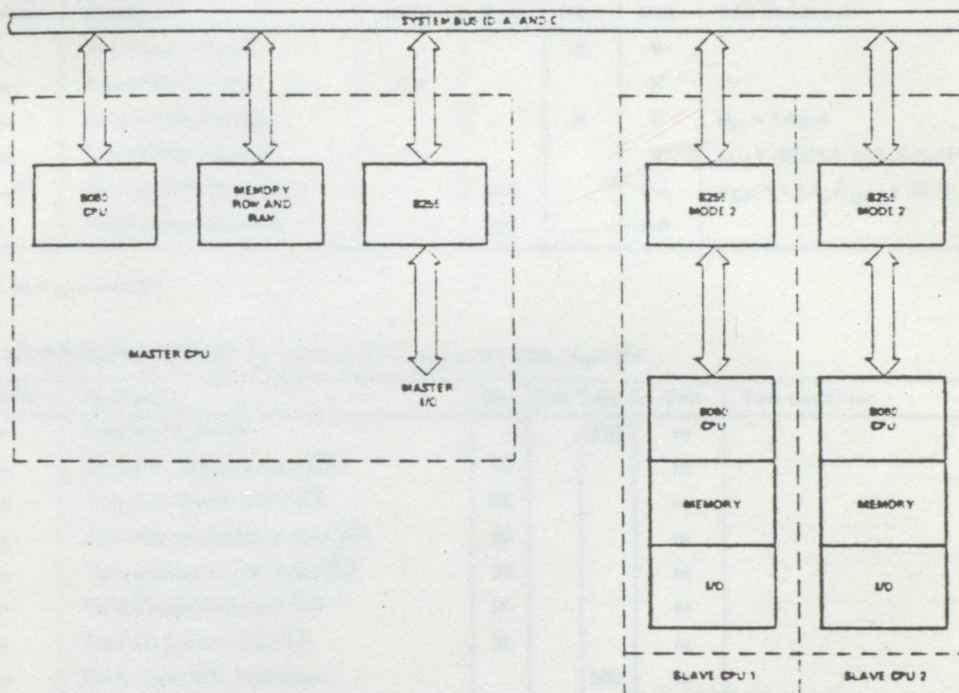
Basic Floppy Disc Interface



Basic CRT Controller Interface

Machine Tool Controller Interface

SILICON GATE MOS 8255



Distributed Intelligence Multi-Processor Interface

SILICON GATE MOS 8255

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = +5V \pm 5\%; V_{SS} = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			.4	V	$I_{OL} = 1.6\text{mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\mu\text{A} (-100\mu\text{A for D.E. Port})$
$I_{OH}^{(1)}$	Darlington Drive Current		2.0		mA	$V_{OH} = 1.5V, R_{EXT} = 390\Omega$
I_{CC}	Power Supply Current		40		mA	

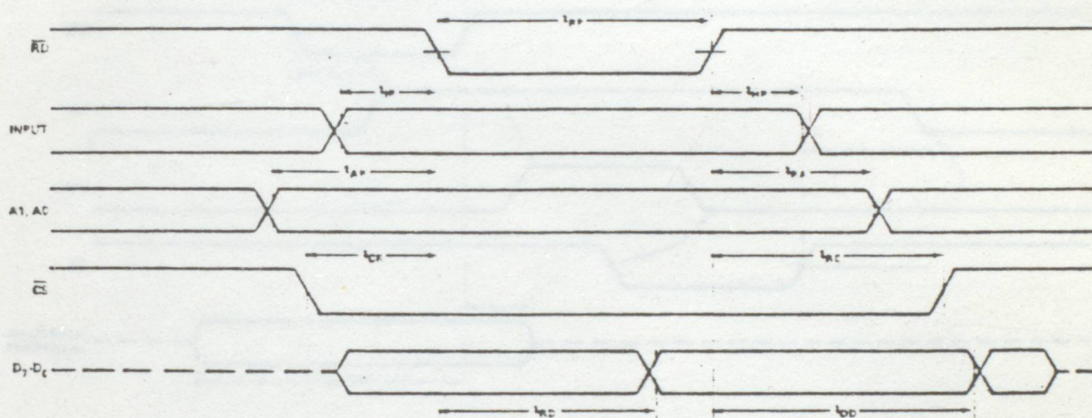
NOTE:

1. Available on E pins only.

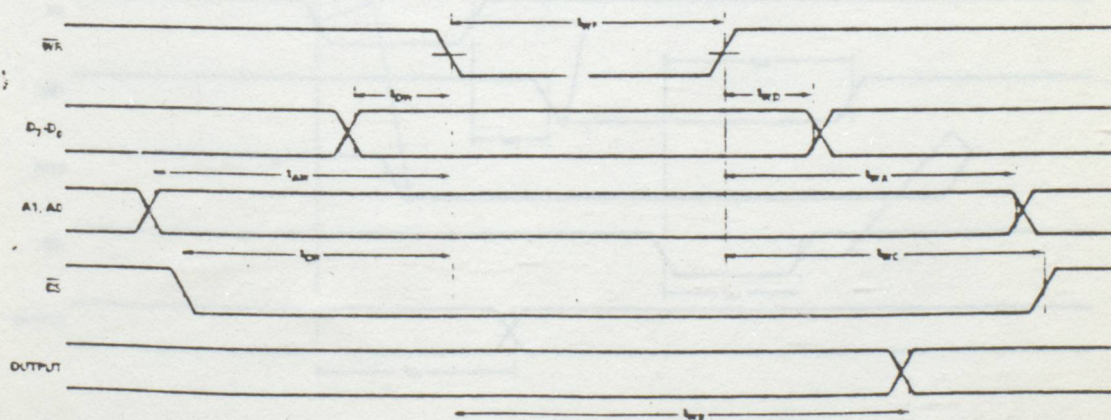
A.C. CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}; V_{CC} = +5V \pm 5\%; V_{SS} = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
t_{WP}	Pulse Width of $\overline{WR}$			430	ns	
t_{DW}	Time D.E. Stable Before $\overline{WR}$	10			ns	
t_{WD}	Time D.E. Stable After $\overline{WR}$	65			ns	
t_{AW}	Time Address Stable Before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable After $\overline{WR}$	35			ns	
t_{CW}	Time CS Stable Before $\overline{WR}$	20			ns	
t_{WC}	Time CS Stable After $\overline{WR}$	35			ns	
t_{WE}	Delay From $\overline{WR}$ To Output			500	ns	
t_{RP}	Pulse Width of $\overline{RD}$	430			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	50			ns	
t_{HR}	Input Hold Time	50			ns	
t_{RD}	Delay From $\overline{RD} = 0$ To System Bus	350			ns	
t_{OD}	Delay From $\overline{RD} = 1$ To System Bus	150			ns	
t_{AR}	Time Address Stable Before $\overline{RD}$	50			ns	
t_{CR}	Time CS Stable Before $\overline{RD}$	50			ns	
t_{AK}	Width Of ACK Pulse	500			ns	
t_{ST}	Width Of STB Pulse	350			ns	
t_{PS}	Set-Up Time For Peripheral	150			ns	
t_{PH}	Hold Time For Peripheral	150			ns	
t_{RA}	Hold Time for A_1, A_0 After $\overline{RD} = 1$	379			ns	
t_{RC}	Hold Time For CS After $\overline{RD} = 1$	5			ns	
t_{AD}	Time From $\overline{ACK} = 0$ To Output (Mode 2)			500	ns	
t_{KD}	Time From $\overline{ACK} = 1$ To Output Floating			300	ns	
t_{WD}	Time From $\overline{WR} = 1$ To $\overline{OBF} = 0$			300	ns	
t_{AD}	Time From $\overline{ACK} = 0$ To $\overline{OBF} = 1$			500	ns	
t_{SI}	Time From $\overline{STB} = 0$ To IBF			600	ns	
t_{RI}	Time From $\overline{RD} = 1$ To IBF = 0			300	ns	

SILICON GATE MOS 8255

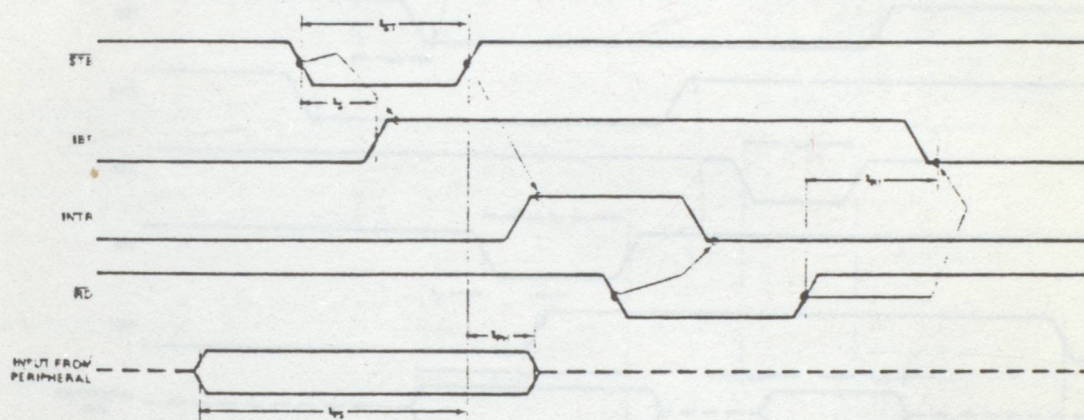


Mode 0 (Basic Input)

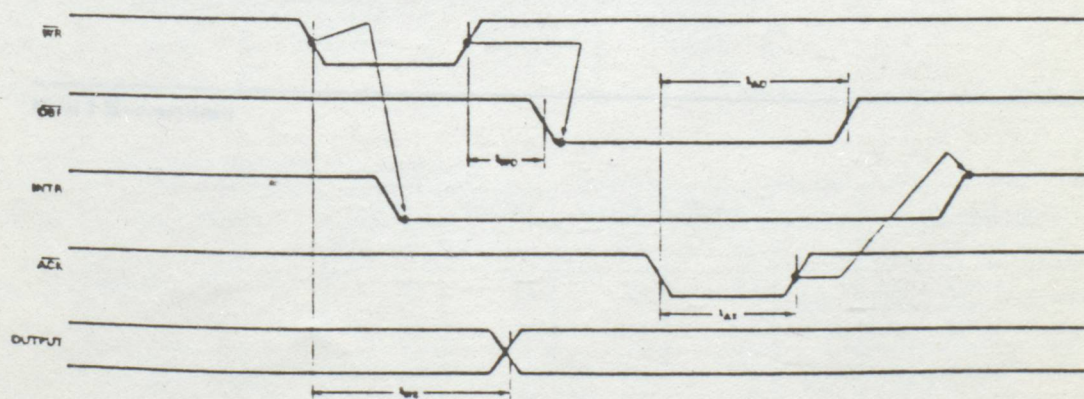


Mode 0 (Basic Output)

SILICON GATE MOS 8255



Mode 1 (Strobed Input)



Mode 1 (Strobed Output)

Mode 2 (Bi-directional)

54/7404
 54H/74H04
 54S/74S04
 54S/74S04A
 54LS/74LS04
 HEX INVERTER

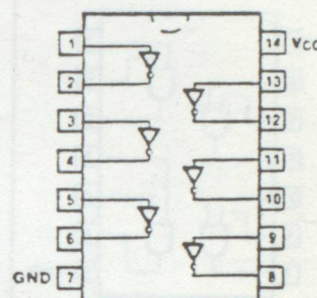
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7404PC, 74H04PC 74S04PC, 74S04APC 74LS04PC		9A
Ceramic DIP (D)	A	7404DC, 74H04DC 74S04DC, 74S04ADC 74LS04DC	5404DM, 54H04DM 54S04DM, 54S04ADM 54LS04DM	6A
Flatpak (F)	A	74S04FC, 74S04AFC 74LS04FC	54S04FM, 54S04AFM 54LS04FM	3I
	B	7404FC, 74H04FC	5404FM, 54H04FM	

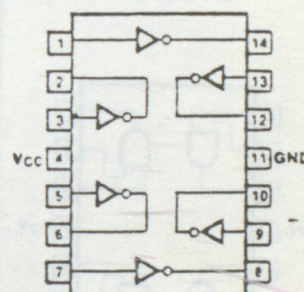
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



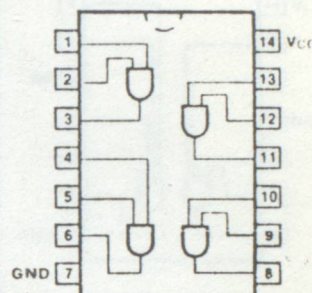
DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max	Min	Max			
ICCH	Power Supply	12		26		24		2.4		mA	VIN = Gnd	VCC = Max
ICCL	Current	33		58		54		6.6			VIN = Open	
tpLH	Propagation Delay	22		10		2.0	4.5	10		ns	Fig. 3-1, 3-4	
tpHL		15		10		2.0	5.0	10				
tpLH	Propagation Delay (54/74S04A only)					1.0	3.5			ns	Fig. 3-1, 3-4	
tpHL						1.0	4.0					

*DC limits apply over operating temperature range. AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

54/7408
54H/74H08
54S/74S08
54LS/74LS08
 QUAD 2-INPUT AND GATE

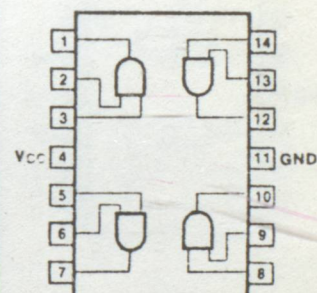
CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7408PC, 74H08PC 74S08PC, 74LS08PC		9A
Ceramic DIP (D)	A	7408DC, 74H08DC 74S08DC, 74LS08DC	5408DM, 54H08DM 54S08DM, 54LS08DM	6A
Flatpak (F)	A	7408FC, 74S08FC 74LS08FC	5408FM, 54S08FM 54LS08FM	3I
	B	74H08FC	54H08FM	

PINOUT B



INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max	Min	Max		V _{IN} = Open	V _{CC} = Max
I _{CCH}	Power Supply	21		40		32		4.8		mA	V _{IN} = Open	
I _{CCL}	Current	33		64		57		8.8			V _{IN} = Gnd	
t _{PLH}	Propagation Delay	27		12		2.5 7.0		13		ns	Fig. 3-1, 3-5	
t _{PHL}		19		12		2.5 7.5		11				

*DC limits apply over operating temperature range. AC limits apply at $T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{ V}$.

54/7421
54H/74H21
54LS/74LS21

DUAL 4-INPUT POSITIVE AND GATE

QUAD 2-INPUT OR GATE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	7421PC, 74H21PC 74LS21PC		9A
Ceramic DIP (D)	A	7421DC, 74H21DC 74LS21DC	5421DM, 54H21DM 54LS21DM	6A
Flatpak (F)	A	7421FC, 74LS21FC	5421FM, 54LS21FM	3I
	B	74H21FC	54H21FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

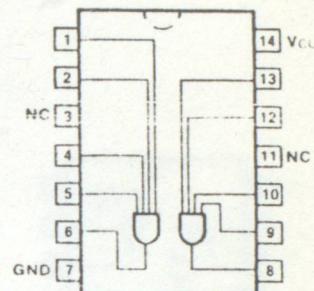
PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

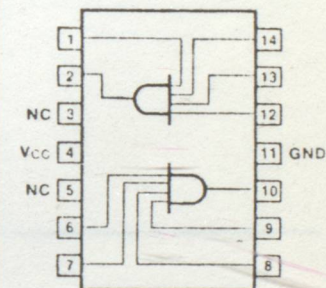
SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max			
I _{CC} H	Power Supply Current	10		20		2.4		mA	V _{IN} = Open	V _{CC} = Max
I _{CC} L		16		32		4.4			V _{IN} = Gnd	
t _{PLH} t _{PHL}	Propagation Delay	27 19		12 12		15 15		ns	Figs. 3-1, 3-5	

*DC limits apply over operating temperature range, AC limits apply at T_A = +25°C and V_{CC} = +5.0 V

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



54/7432
54S/74S32
54LS/74LS32
QUAD 2-INPUT OR GATE

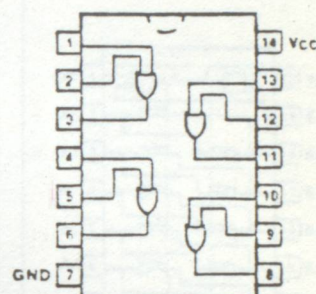
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAM
PINOUT A



DC AND AC CHARACTERISTICS: See Section 3 for U.L. definitions

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max			
I _{CC} H	Power Supply Current	22		32		6.2		mA	V _{IN} = Open	V _{CC} = Max
I _{CC} L		38		68		9.8			V _{IN} = Gnd	
t _{PLH} t _{PHL}	Propagation Delay	15	2.0 7.0	15		15		ns	Figs. 3-1, 3-5	
		22	2.0 7.0	15		15				

*DC limits apply over operating temperature range, AC limits apply at $T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0 \text{ V}$.

54LS/74LS245

OCTAL BUS TRANSCEIVER

(With 3-State Outputs)

DESCRIPTION — The 'LS245 is an octal bus transmitter/receiver designed for 8-line asynchronous 2-way data communication between data busses. Direction input (DR) controls transmission of data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\bar{E}$) can be used to isolate the busses.

- HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

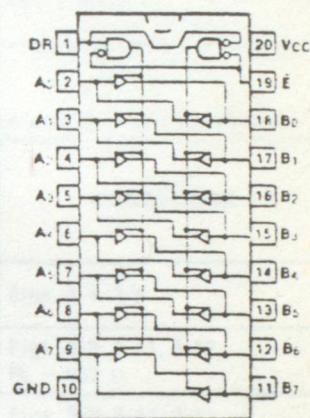
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS245PC		9Z
Ceramic DIP (D)	A	74LS245DC	54LS245DM	4E
Flatpak (F)	A	74LS245FC	54LS245FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS		UNITS	CONDITIONS	
			Min	Max			
VOH	Output HIGH Voltage	XM	2.0		V	IOH = -12 mA	VCC = Min VIN = VIH or VIL per Truth Table
		XC	2.0			IOH = -15 mA	
VOH	Output HIGH Voltage		2.4		V	IOH = -3.0 mA, VCC = Min VIN = VIH or VIL per Truth Table	
VT+ — VT-	Hysteresis Voltage		0.2		V	VCC = Min	
IOS	Output Short Circuit Current		-40	-225	mA	VCC = Max, VOUT = 0 V	
ICC	Power Supply Current	HIGH		70	mA	VCC = Max	
		LOW		90			
		OFF		95			

AC CHARACTERISTICS: VCC = +5.0 V, TA = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C _L = 45 pF			
		Min	Max		
t _{PLH} t _{PHL}	Propagation Delay Data to Output		18 18	ns	Figs. 3-1, 3-5
t _{PZH} t _{PZL}	Output Enable Time		25 30	ns	Figs. 3-3, 3-11, 3-12 R _L = 667 Ω
t _{PLZ} t _{PHZ}	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R _L = 667 Ω, C _L = 5 pF

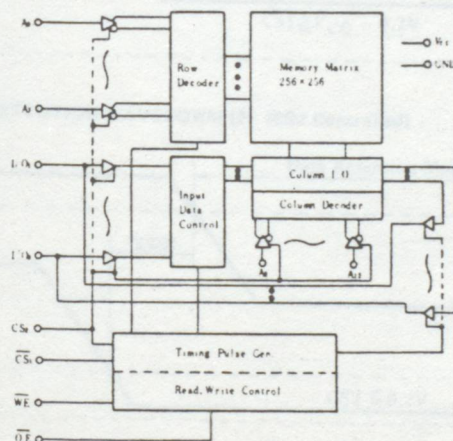
HM6264LP-10, HM6264LP-12 HM6264LP-15

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.01mW (typ.)
- Low Power Operation Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

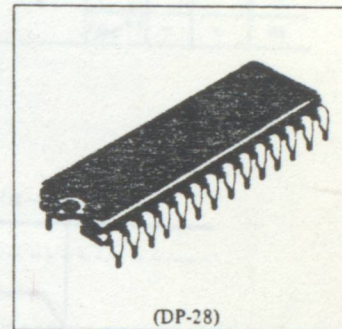
Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

* With respect to GND. ** Pulse width 50ns: -3.0V

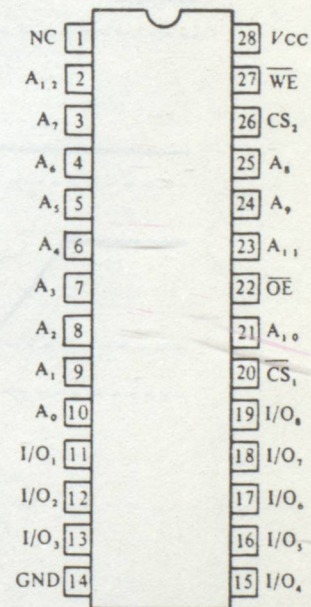
■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L	Write	Din	I_{CC}, I_{CC1}	Write Cycle (2)

* : Don't care.



■ PIN ARRANGEMENT



(Top View)

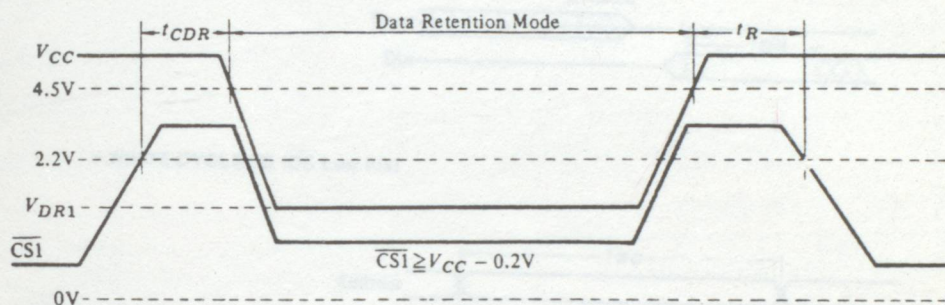
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2\text{V}, CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$	2.0	—	—	V
	V_{DR2}	$CS2 \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0\text{V}, \overline{CS1} \geq V_{CC} - 0.2\text{V}, CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$	—	1	50*	μA
	I_{CCDR2}	$V_{CC} = 3.0\text{V}, CS2 \leq 0.2\text{V}$	—	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^{**}	—	—	ns

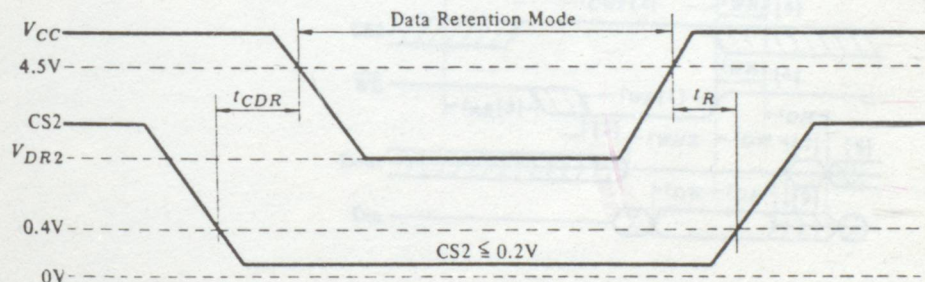
* $V_{IL \text{ min}} = -0.3\text{V}$

** t_{RC} = Read Cycle Time

• LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

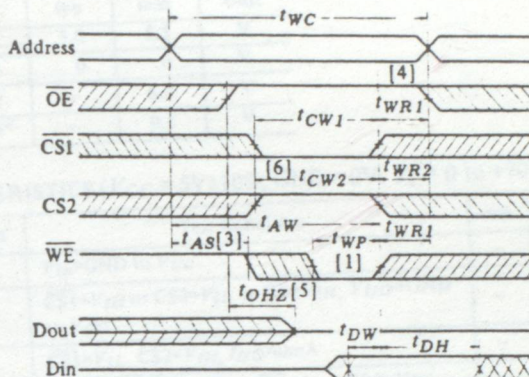


• LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)

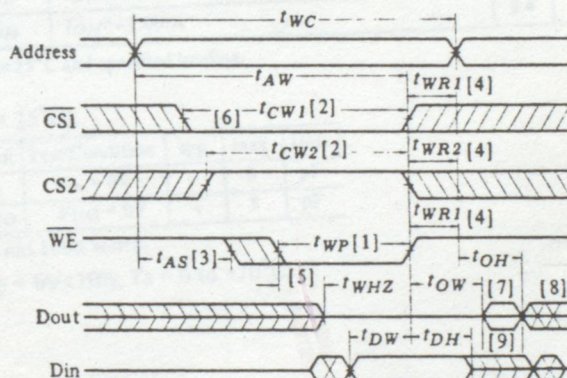


NOTE: CS_2 controls Address buffer, $\overline{WE}$ buffer, $\overline{CS}$, buffer and Din buffer. If CS_2 controls data retention mode, V_{in} level (Address, $\overline{WE}$, $\overline{CS}$, I/O) can be in the high impedance state. If $\overline{CS}$ controls data retention mode, CS_2 must be $CS_2 \geq V_{CC} - 0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$. The other inputs level (address, $\overline{WE}$, I/O) can be in the high impedance state.

• WRITE CYCLE (1) ($\overline{\text{OE}}$ clock)



• WRITE CYCLE (2) ($\overline{\text{OE}}$ Low Fix)



- NOTES:
- 1) A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high $\overline{\text{CS2}}$ and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, $\overline{\text{CS2}}$ going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, $\overline{\text{CS2}}$ going low and $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 - 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or $\overline{\text{CS2}}$ going high to the end of write.
 - 3) t_{AS} is measured from the address valid to the beginning of write.
 - 4) t_{WR} is measured from the end of write to the address change.
 - t_{WR1} applies in case a write ends at $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.
 - t_{WR2} applies in case a write ends at $\overline{\text{CS2}}$ going low.
 - 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 - 6) If $\overline{\text{CS1}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
 - 7) D_{out} is in the same phase of written data of this cycle.
 - 8) D_{out} is the read data of the new address.
 - 9) If $\overline{\text{CS1}}$ is low and $\overline{\text{CS2}}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.3*	—	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	I_{L1}	$V_{in} = \text{GND to } V_{CC}$	—	—	2	μA
Output Leakage Current	I_{LO}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\text{OE} = V_{IH}$, $V_{I/O} = \text{GND to } V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	—	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$	—	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$, $I_{I/O} = 0\text{mA}$	—	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	—	2	100	μA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	—	2	100	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

** V_{IL} min = -0.3V

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	—	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

• AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

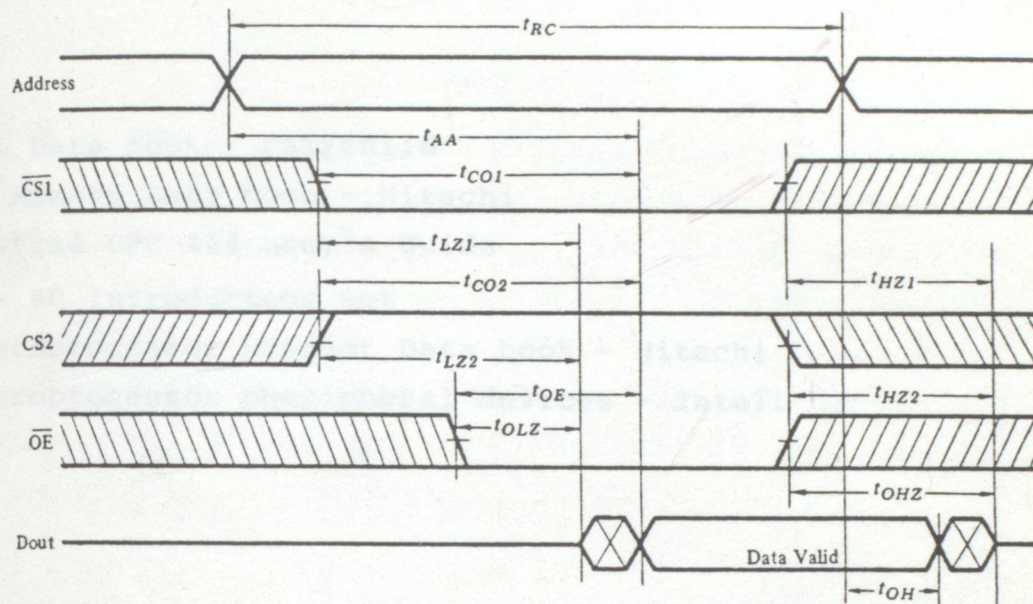
Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	—	120	—	150	—	ns
Address Access Time		t_{AA}	—	100	—	120	—	150	ns
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	—	100	—	120	—	150	ns
	CS2	t_{CO2}	—	100	—	120	—	150	ns
Output Enable to Output Valid		t_{OE}	—	50	—	60	—	70	ns
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	—	10	—	15	—	ns
	CS2	t_{LZ2}	10	—	10	—	15	—	ns
Output Enable to Output in Low Z		t_{OLZ}	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	—	10	—	15	—	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE



NOTE : 1) $\overline{WE}$ is high for Read Cycle

• WRITE CYCLE

Item	Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	80	—	85	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	80	—	85	—	100	—	ns
Write Pulse Width	t_{WP}	60	—	70	—	90	—	ns
Write Recovery Time	CS1, $\overline{WE}$	t_{WR1}	5	—	5	—	10	ns
	CS2	t_{WR2}	15	—	15	—	15	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	10	—	ns

K A Y N A K L A R

- TTL Data book - Fairchild
- IC Memory Data book - Hitachi
- Amstrad CPC 464 User's Guide
- Z - 80 Introduction set
- Microprocessör product Data book - Hitachi
- Microprocessör pheripheral devices - Intel.

Ö Z G E Ç M İ Ş

Fatih Şimşek 1963 yılında Zonguldak ilinde doğdu.. İlk, Orta ve Lise öğrenimini Zonguldak Mehmet Çelikel Lisesinde tamamladı. 1981 yılında girdiği Yıldız Üniversitesi Elektronik ve Haberleşme Mühendisliği bölümünden 1985 yılında mezun oldu. Aynı yıl bölümünde Lisans Üstü eğitimine başladı. 1985 yılından beri NET Turistik tesisler A.Ş.'de Teknik Servis Şefi olarak çalışmaktadır.

